



GS12090

Design Guide

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
0	033829	—	October 2016	New Document.

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General Description

The GS12090 is a high performance UHD-SDI re-timing configurable adaptive cable equalizer and cable driver. This Design guide is intended to be a product specific addendum to the GS121x1 Design Guide (PDS-060957). It provides useful guidelines for designing an effective power distribution network for the GS12090. In addition to the power distribution network, proper layout of high speed lines for optimal signal integrity and performance is also required.

Pinout

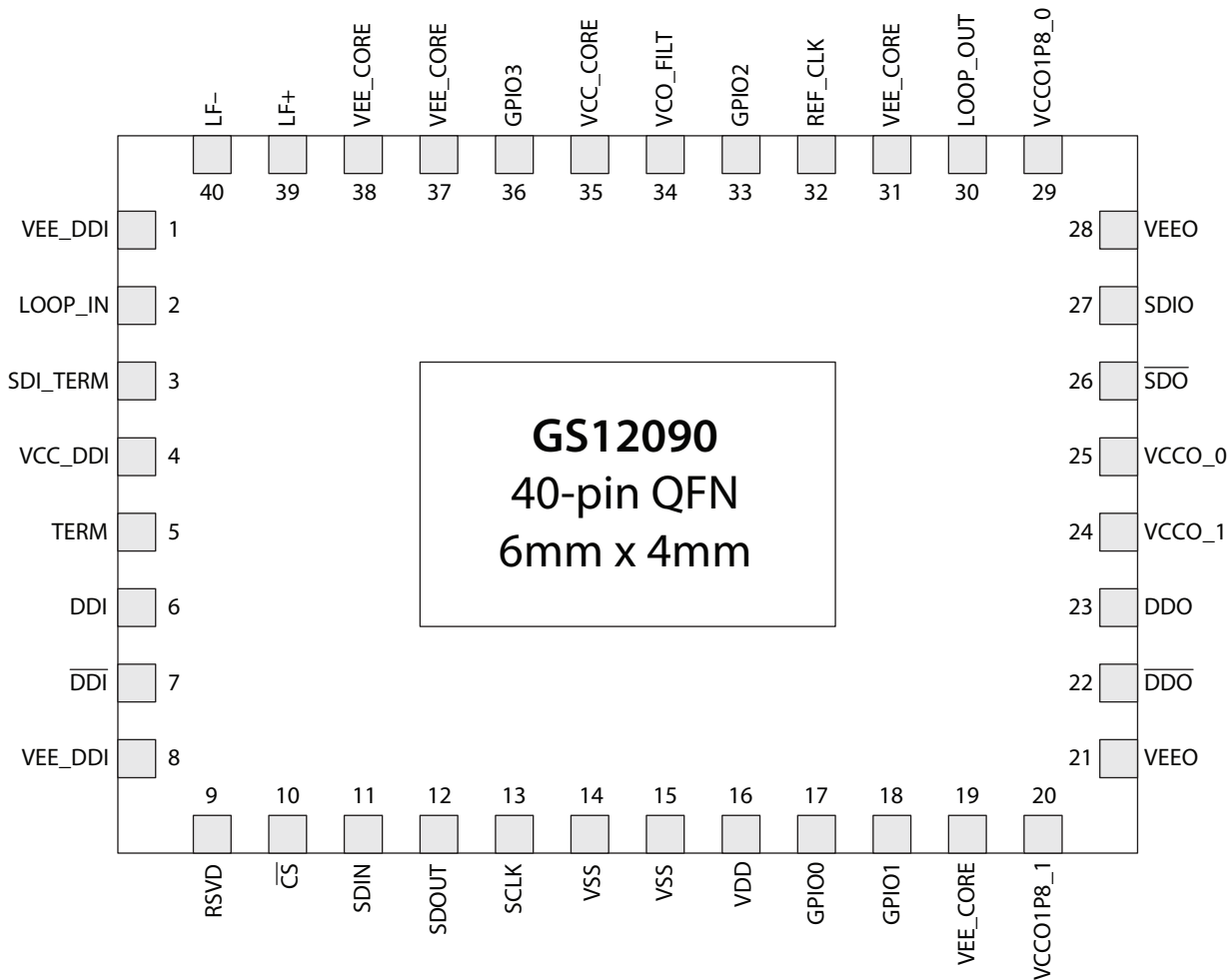


Figure A: GS12090 Pinout

Typical Application Circuit

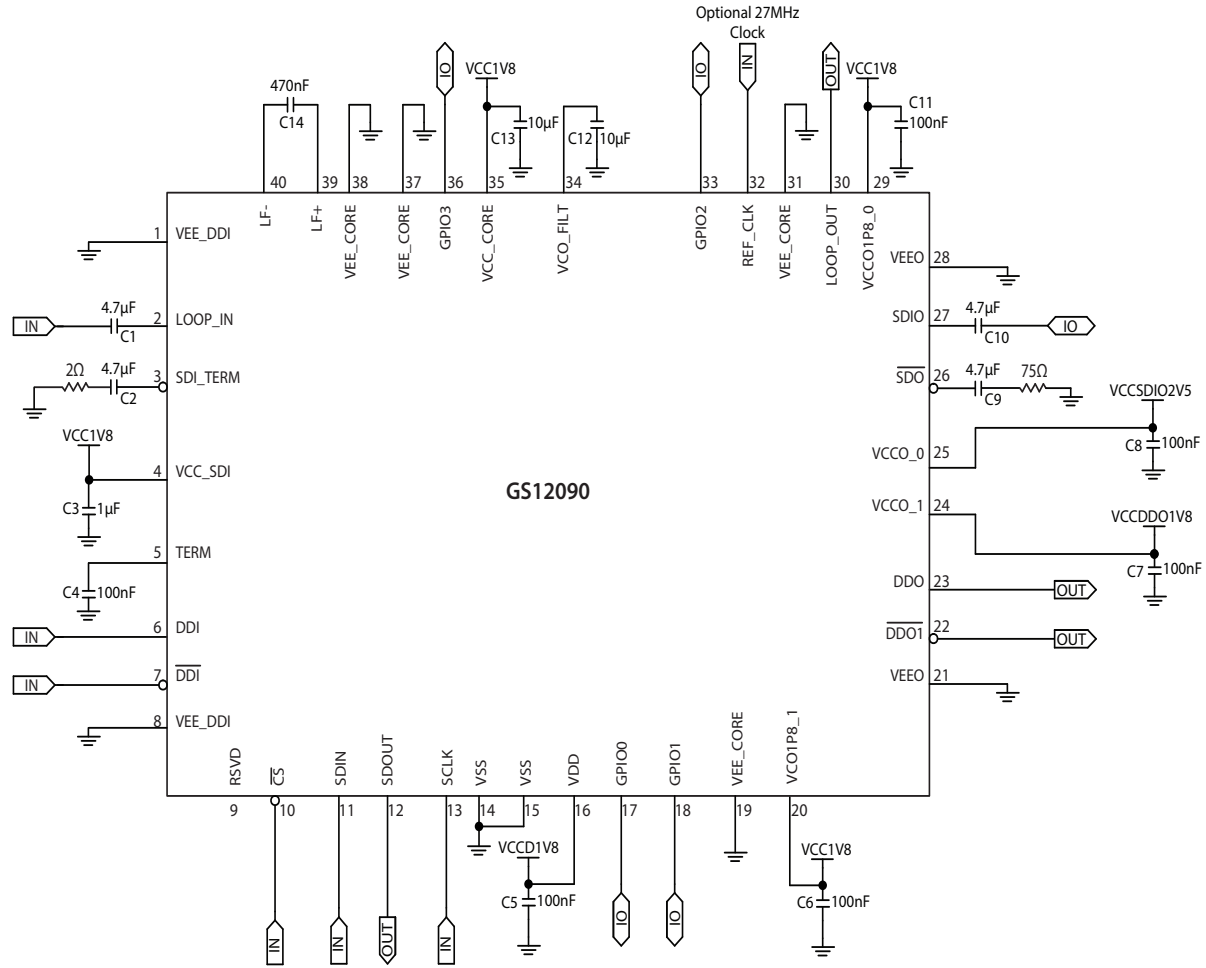


Figure B: Typical Application Circuit

Power

The core supplies of the GS12090 are 1.8V, while the output supplies can be configured to meet the application interface requirements. The details of the supplies are as follows:

VCC_SDI, VCC_CORE, VDD, VCCO1P8_0, and VCCO1P8_1 are mandatory 1.8V supplies.

VCCO_0 is the supply for the configurable 75Ω port and can be 2.5V or 3.3V, however 2.5V is recommended.

VCCO_1 is the supply for the trace driver output and can be 1.2V, 1.8V, or 2.5V. The selection of supply voltage for the trace driver can be made to facilitate DC coupling to the downstream device input.

The supplies should be isolated from each other in the following groups:

Group1: (VCC_CORE, VCC_SDI)

Group2: (VCCO1P8_0, VCCO1P8_1, VDD)

Group3: (VCCO_0)

Group4: (VCCO_1)

Note1: Group 1, 2, 3, and 4 should have filtered supply to main rails. Switching supplies may be used if ripple at decoupled pin can be kept under < 1%. This may require additional decoupling capacitors

Note2: If multiple devices are to be designed on the same board, one filtered plane per group may be used.

Decoupling

It is recommended to place the main decoupling capacitors on the top side to minimize loop inductance. Since not all PDNs have the same characteristics, additional decoupling may be beneficial. Any additional decoupling may be placed on the bottom side of the board.

The VCC_CORE and VCO_FILT pins (35 and 34), require 10μF decoupling capacitors. Adding smaller capacitors such as 10nF and 100nF are not required, but may be added on the top or bottom. If 0201 components are allowed, room may be available on the top side of the board.

- The ground connection for the decoupling capacitor of pin 35 should be directly connected to pin 38.
- The ground connection for the decoupling capacitor of pin 34 should be directly connected to pin 31.
- The ground connection for the decoupling capacitor of pin 29 should be directly connected to pin 28.
- The ground connection for the decoupling capacitor of pin 20 should be directly connected to pin 21.
- The ground connection for the decoupling capacitor of pin 16 should be directly connected to pin 14.
- The ground connection for the decoupling capacitor of pin 34 should be directly connected to pin 31.

Layout Considerations

The layout of the GS12090 is straight forward. The High speed traces should follow recommended practices for high speed design. See the GS121x1 Design Guide (PDS-060957) for detailed information.

For the GS12090 in Particular, the loopback trace from pin 30 to pin 2 must be carefully laid out as a 75Ω transmission line with antipad under AC coupling capacitor.

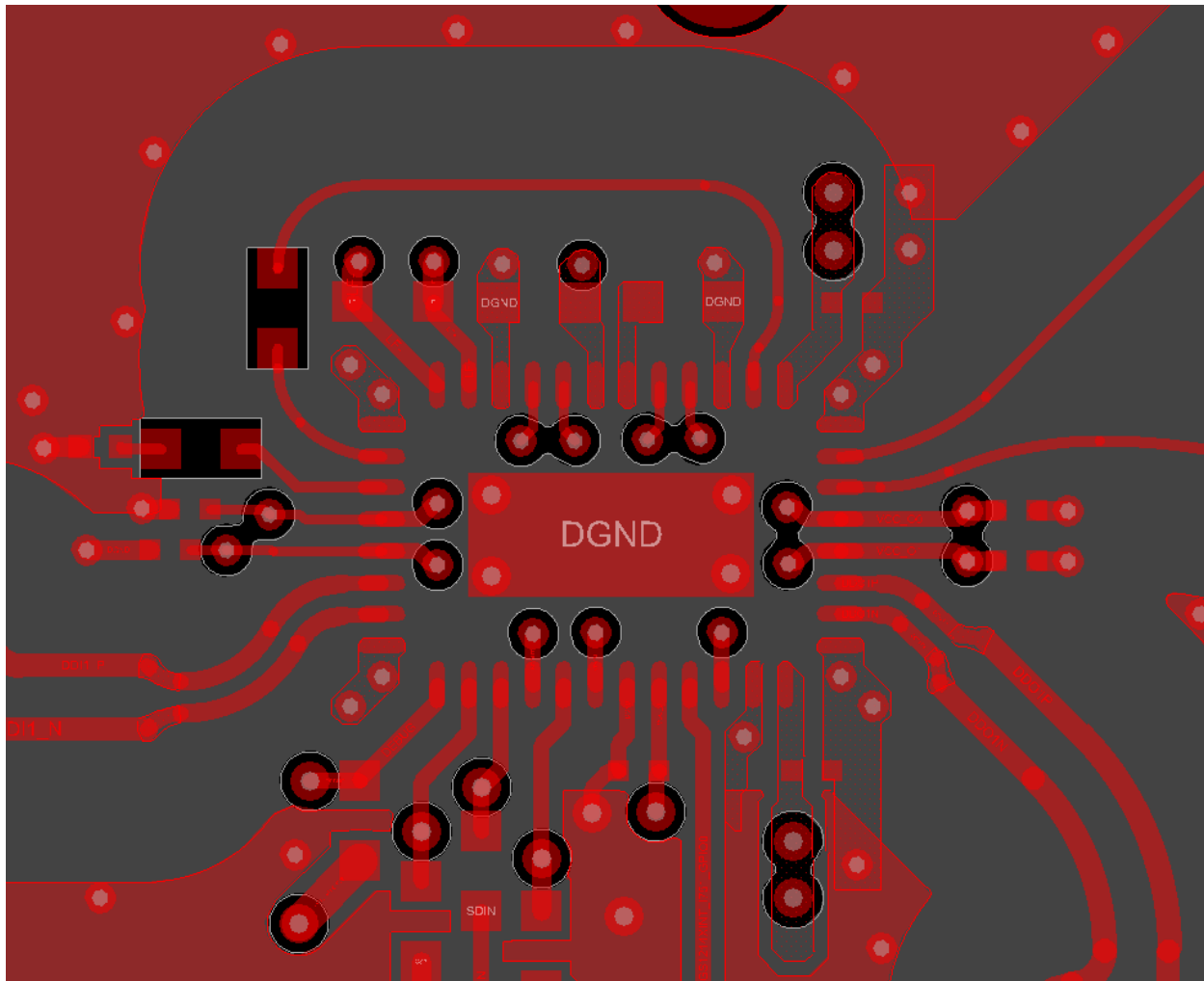


Figure C: GS12090 Typical Layout with 0402 and 0201 Components



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