GS12070 UHD-SDI Gearbox

Design Guide

Revision History

Version	ECO	Date	Changes and/or Modifications
2	040962	February 2018	Updated Section 1.2, Figure 3-1 and Figure 3-2.
1	040323	January 2018	Updates throughout.
0	032774	September 2016	New document.

Contents

Overview

This document is intended to aid in the hardware design and implementation of a system integrating the GS12070 UHD-SDI Gearbox. This document should be used along with the GS12070 Data Sheet and other relevant User Guides and Application Notes.

In addition to this Design Guide, the following resources are available when designing with the GS12070:

- GS12070 Data Sheet (PDS-061012)
- Reference Design Kit (RDK-GS12070-XX) with Design Schematic and Layout
- RDK User Guide (PDS-061370)
- Application Notes

In multi-GHz systems, issues such as channel losses, reflections and cross-talk, clock routing and power distribution represent significant design challenges. In the case of the GS12070, the main focus areas are:

- Reference clock crystal
- Power supply distribution
- High-speed serial interfaces (DDI[3:0] and DDO[3:0])
- Thermal considerations

1. Design Considerations

1.1 DDI and DDO Interfaces

1.1.1 High-Speed Serial Inputs

The GS12070 has four serial inputs which are capable of handling data rates from 270Mb/s to 11.88Gb/s. The GS12070's inputs feature a differential input buffer with 100Ω differential input termination, which includes an adaptive Trace Equalizer.

It is mandatory to use AC-coupling capacitors on these inputs. A 4.7µF capacitor value is recommended.

For 12Gb/s data rates, the Trace Equalizer is adaptive within three specific channel loss bands:

- 0dB to 4dB
- 4dB to 8dB
- 8dB to 12dB

For all other data rates, the Trace Equalizer is adaptive within 0dB to 12dB of loss.

Upon initialization, the selection of these ranges needs to be programmed via the GS12070 host interface. For specific values, refer to Section 3.2.2 (Input Trace Equalization) in the Data Sheet.

If the connection to this device results in losses greater than the loss compensation capability shown above, lower loss board materials can be considered. Alternatively, if the device driving the serial inputs has pre-emphasis/boost capabilities, this can be used to augment the loss compensation of the serial inputs.

Input traces should be routed as 100Ω differential traces.

1.1.2 High-Speed Serial Outputs

The GS12070 has four differential outputs (DDO) which are capable of handling data rates from 270Mb/s to 11.88Gb/s.

The differential outputs can be DC-coupled to downstream devices, provided they meet the common-mode of the serial output drivers. Alternatively, outputs can be AC-coupled using 4.7µF capacitors.

Each serial output buffer includes a de-emphasis circuit that can be independently configured to address signal integrity issues and improve the high-speed signal quality.

For further details regarding the de-emphasis feature, please refer to the *Using the GS12070 UHD-SDI Gearbox De-Emphasis Feature* (PDS-061520) Application Note.

1.2 Reference Inputs

The GS12070 operates from a single reference clock. It is recommended to use a crystal with ±30ppm frequency tolerance or better, with a temperature range of -40°C to +85°C and load capacitance of 8pF to 18pF. A 27MHz crystal can be connected to XTAL_IN/OUT as shown in Figure 1-1.

When a 27MHz crystal is used as reference, the REFCLK_SEL[1:0] reference clock configuration selection pins should be grounded. REF_IN/OUT pins should be left unconnected.

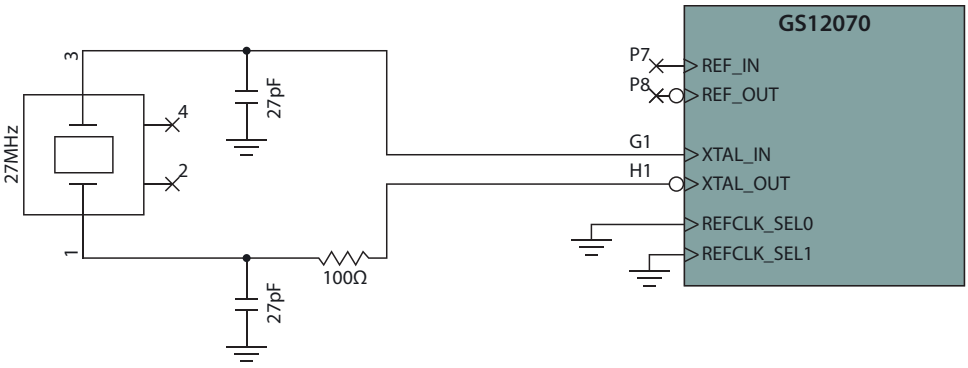


Figure 1-1: GS12070 Reference Crystal Schematic

Crystal Examples:

- NDK America, Inc. #NX3225SA-27M-STD-CRS-2 (used over temperature performance characterization)
- Abracon #ABM8G-27.000MHZ-18-D2Y-T (used on the RDK-GS12070)

As an alternative to using the crystal, a differential clock can be used and connected to the XTAL_IN/OUT pins. When a differential clock is used as a reference, the REFCLK_SEL[1:0] reference clock configuration selection pins should be set to 01_b. The REF_IN/OUT pins should be left unconnected. The quality of this reference clock must be equivalent or better than the crystal as it will impact the output jitter. The differential clock must be AC-coupled with a 10nF capacitor. The amplitude should be LVDS/CML compatible (800mV$_{pp}$ to 1600mV$_{pp}$ with AC-coupling).

1.3 Power Supply Partitioning and Filtering

The GS12070 has four power supplies that can be connected to three separate power supply rails:

- The high-speed analogue power supply (1.8V)
  - VCC_A_1V8
  - This supply should be filtered or supplied from a clean source
- The digital and analogue core supply (1.1V)
  - VCC_A_1V1, VCC_CORE
  - These supplies can be connected together to one voltage source
- The digital I/O supply (1.8V)
  - VCC_IO
  - This supply can be shared with the rest of the system

Bulk decoupling (470nF/4.7µF/100µF) is recommended at the power entry point and local decoupling capacitors (10nF) are strongly recommended at each of the power supply pins. For application circuits, please refer to Section 3.

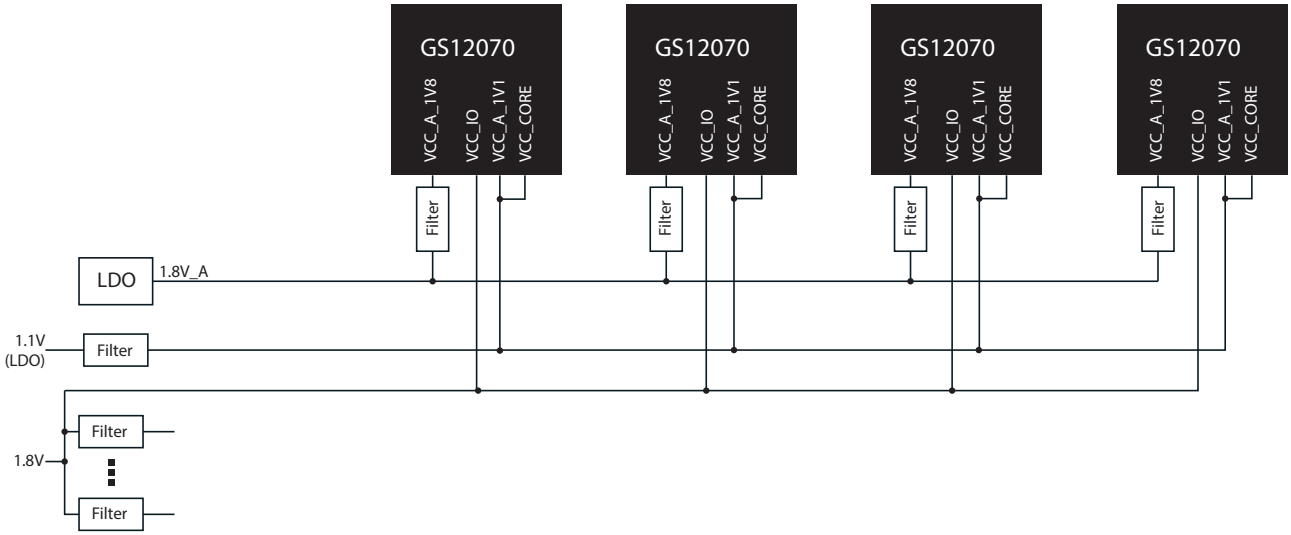


Figure 1-2: Recommended Power Supply Partitioning

As an example: The RDK-GS12070 uses Semtech's SC414 integrated FET regulator and SC4216 very low input/dropout regulators.

1.4 Unused Pins

Some designs will only require a subset of features of the GS12070. The following pins can be left unconnected if the respective feature is not used:

- Unused DDI/$\overline{\text{DDI}}$ Inputs
- Unused DDO/$\overline{\text{DDO}}$ Outputs
- REF_IN/REF_OUT
- TX_PCLK[1:0]
- RX_CLK[3:0]
- JTAG pins
- STAT[15:0]
- TIM_OUT[3:0]

In addition, if control inputs are left unconnected, internal pull-ups or pull-downs will determine the default state. Please refer to the pin description table in the GS12070 Data Sheet.

Note: RSVD and NC pins must be left unconnected.

1.5 REXT_RX

A 33pF capacitor parallel to the calibration resistor on REXT_RX is recommended to filter any noise on this sensitive analogue pin. The resistor and capacitor should be placed as close as possible to the REXT_RX pin. For a layout example please refer to Figure 2-2.

2. Layout Considerations

2.1 High-Speed I/O and Reference Clock Routing

The DDI and DDO differential input and output package balls, as well as the XTAL_IN/XTAL_OUT balls, have been placed on the periphery of the device. This configuration avoids having to route between balls, or having to transition layers (using vias) for the high-speed transmission lines. In addition, the ball-out facilitates the best compromise between input and output signals sourced from one side of the PCB or from opposite sides.

Impedance of the differential high-speed lines needs to be controlled at 100Ω ±10%. It is recommended to couple them with the nearest ground plane.

Figure 2-1 below shows an example of routing high-speed lines, using the Reference Design Board layout (RDK-GS12070-XX).

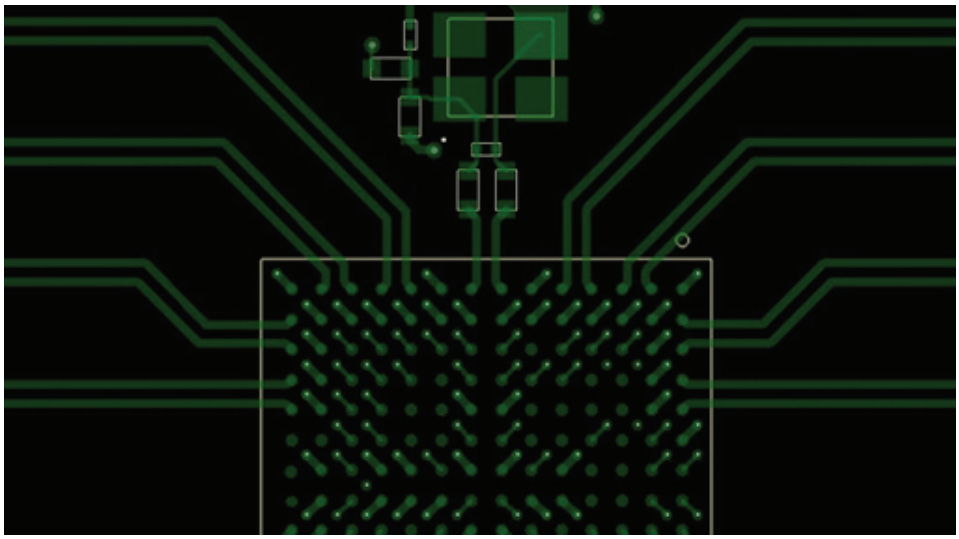


Figure 2-1: GS12070 Layout Example (high-speed lines top layer)

2.2 Decoupling Capacitor Placement

Board decoupling and efficient placement of local power supply decoupling capacitors is important for improving overall power supply integrity while ensuring the rated device performance.

In order to minimize the inductance path created, decoupling capacitors should be placed as close as possible to the BGA pads, maintaining the shortest possible distance between the two. This is accomplished by having decoupling capacitors placed between vias connected to the device's power and corresponding ground pins. It is recommended to place one 10nF decoupling capacitor for each power ball, on the bottom side of the PCB underneath their corresponding power connections, and as close as possible to the via/BGA pad. Decoupling capacitors should not share ground vias. One decoupling capacitor should be connected to one ground via on the bottom layer, which is connected to the ground ball on the top layer.

Decoupling capacitor footprint pads are designed to fit over the BGA vias as can be seen in the layout example in Figure 2-2. In this layout example, only 0402 footprints have been used.

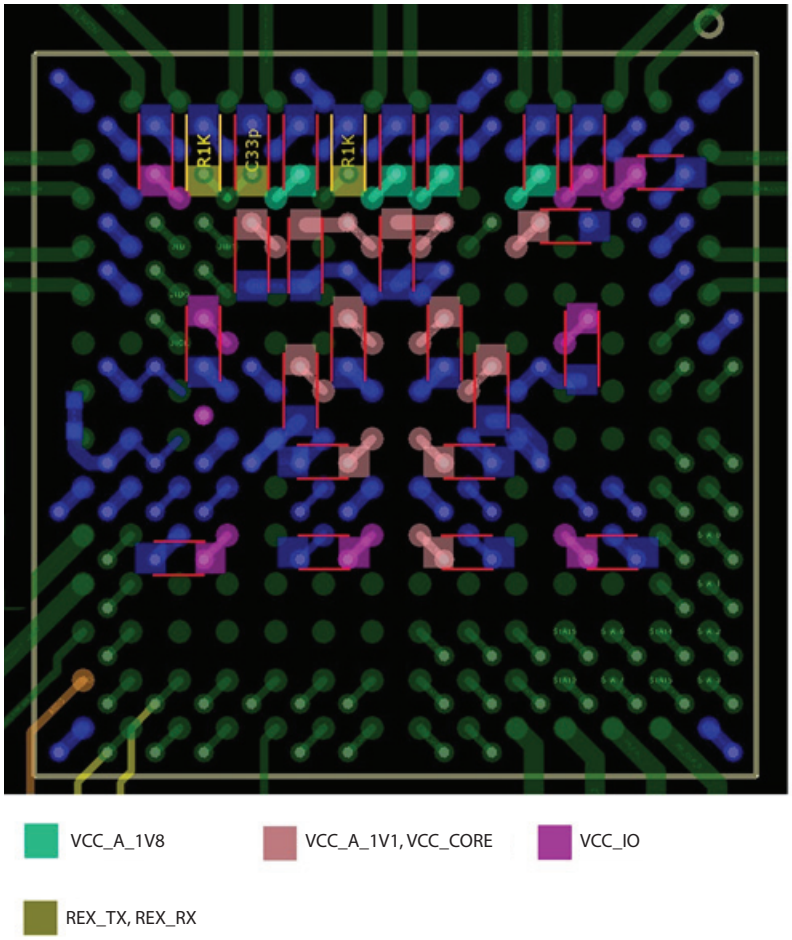


Figure 2-2: GS12070 Layout Example (placement of decoupling capacitors on the bottom layer)

The GS12070 package substrate was designed to provide optimal placement of decoupling capacitors. However, this design trade-off resulted in the following decoupling capacitor placement requirements, as shown in the above example:

- Two VCC_A_1V1 decoupling capacitors share the same GND (connected to K4 and H4)
- One VCC_A_1V1 capacitor (E4) connects to the GND via that is not connected to the device's ground ball

2.3 Stack-Up and Materials

The RDK-GS12070-XX has all high-speed DDI/DDO signals routed on layer one, which is constructed of an FR4 core.

When designing the board stack-up, a choice must be made between core layers or prepreg and foil layers. PCB cores are manufactured according to published specifications. Prepreg (and foil, if necessary) layers are inserted and stacked-up as required by the PCB fabricator, making for a less-controlled PCB.

A core is used to ensure a consistent dielectric value across the high-speed transmission sections. Cores are used in other layers to improve board consistency and reduce defects such as warping and bowing. The bottom layer also uses a FR4 core layer for board consistency, but does not contain any high-speed routing.

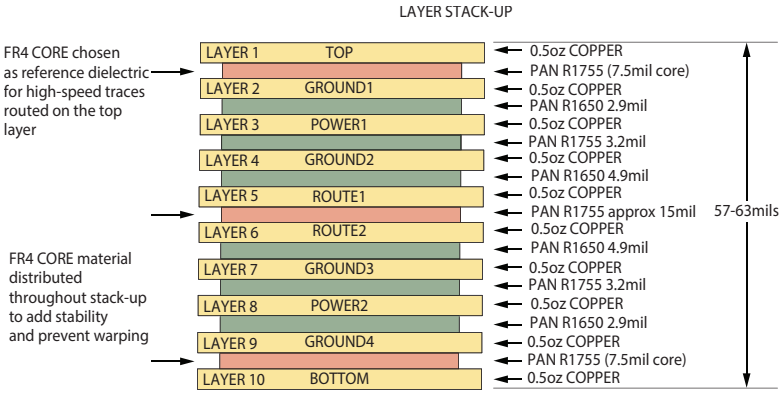


Figure 2-3: RDK-GS12070-XX Reference Design Board Stack-Up

As an example, Figure 2-3 shows the stack-up used for the RDK-GS12070-XX reference design board.

Board materials such as Panasonic R1755, R1650 and ISOLA 370HR are considered as similar materials and are often interchanged by fabricators. These materials are referred to as “FR4” and are suitable materials for GS12070 systems where dielectric loss due to very long traces is not an issue. If very long high-speed transmission lines are required, lower loss dielectrics such as ISOLA FR408 may be more appropriate. FR408 has higher performance than FR4 materials, specifically, a lower and more stable dielectric constant over frequency.

2.3.1 Power Planes

It is recommended that wherever possible, stack-ups be designed so that power and ground planes are tightly-coupled to provide additional evenly-distributed decoupling capacitance. The RDK board has two power layers: layer 3 and layer 8. Layer 3 is tightly-coupled to ground layers 2 and 4. Similarly, layer 8 power is tightly-coupled to ground layers 7 and 9. Power and ground planes form a natural capacitor, which will increase the total decoupling capacitance.

Power and ground planes should be placed near the component side of the board to reduce the inductance of vias connecting the device to the reference planes. This also has the added benefit of improving crosstalk.

2.4 Thermal Considerations

The GS12070 does not require a heat sink. To ensure the GS12070's rated performance over a specified ambient temperature range, common thermal design practices when designing with flip-chip devices should be followed.

The majority of the heat (80%) generated in the GS12070 die is conducted through the substrate into the PCB and radiated through it; around 20% of the heat is radiated directly from the die and substrate into the air.

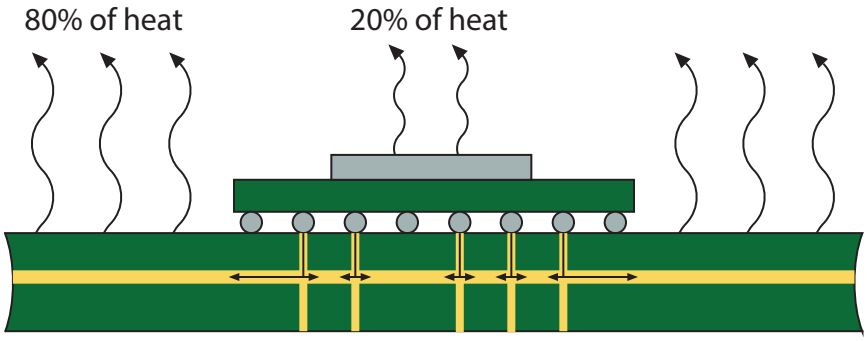


Figure 2-4: GS12070 Heat Flow

The number one thermal enhancement when designing with a flip-chip BGA package is an appropriate number of well-designed thermal vias. These thermal vias are most effective when attached to a large plane in the PCB (for example, ground or power), with an adequate area to ventilate the heat from the component to the environment.

Below are a few strategies to improve heat dissipation from the GS12070 into the PCB:

- Using 1oz copper weights instead of 0.5oz for power and ground planes can help increase heat transferred and dissipated through the PCB
- Sharing of vias between adjacent ground and power pins should be avoided as it reduces the amount of heat transferred to the board
- Use BGA vias as large as the design allows—the GS12070 RDK uses 14/8 vias
- Using a stack-up with multiple ground layers where possible and appropriate number of stitching vias provides additional heat sinking

Other factors when analysing thermal performance are system-level requirements. Factors that may influence thermal flow at system-level must be taken in account, such as:

- Number of neighbouring devices
- Airflow
- Location on the PCB
- Ambient temperature conditions

3. Appendix

3.1 Application Diagrams

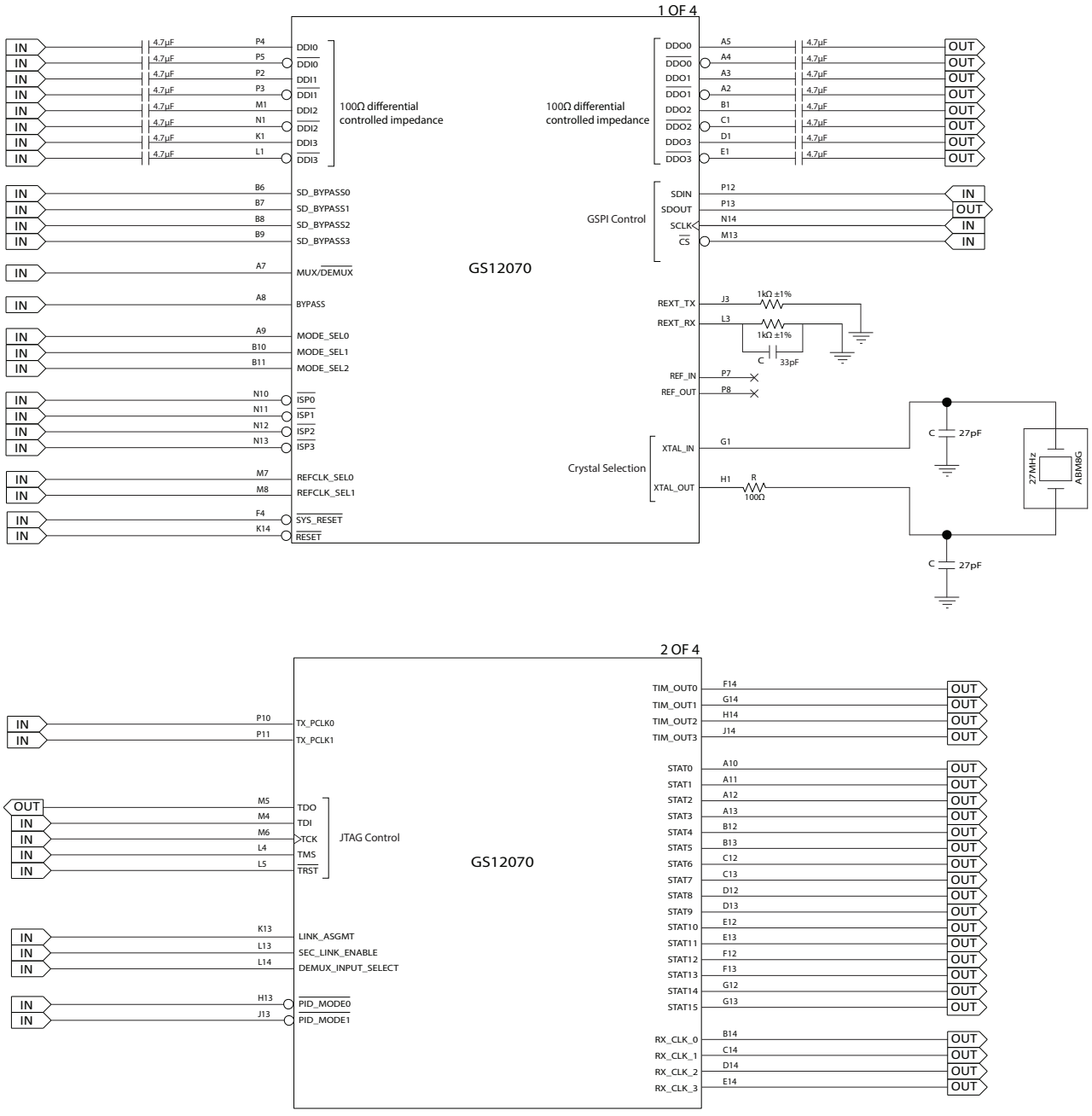
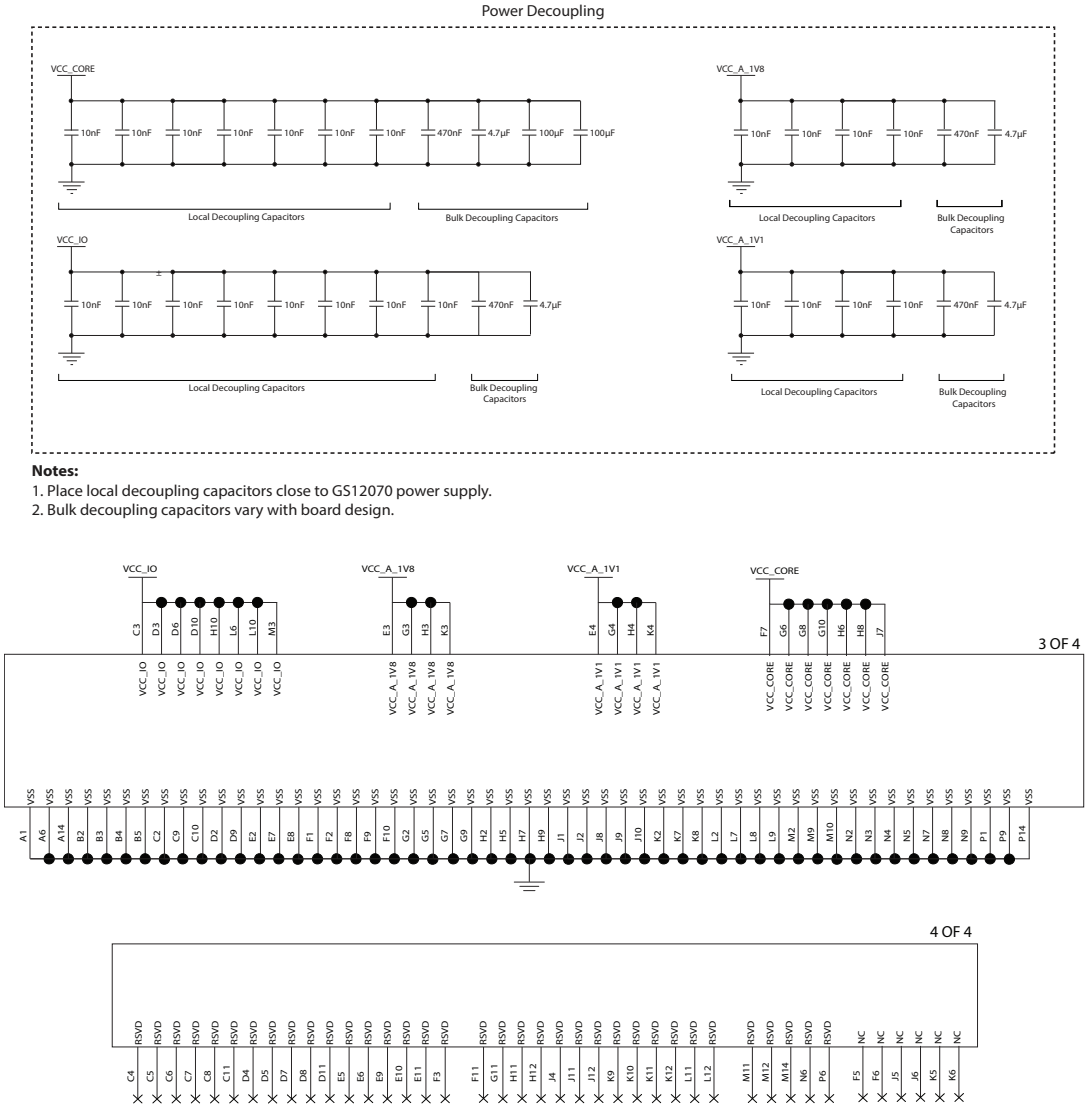


Figure 3-1: GS12070 Typical Application Schematic 1

Note: The capacitor on REXT_RX is recommended to filter any noise on the sensitive analog pin.



Notes:

1. Place local decoupling capacitors close to GS12070 power supply.
2. Bulk decoupling capacitors vary with board design.

Figure 3-2: GS12070 Typical Application Schematic 2

Contact Information

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