

**PROTECTION PRODUCTS**
**PCB Design Guidelines for ESD Suppression**

Printed circuit board (PCB) layout is a critical component for ESD immunity. Initial effort invested in a sound PCB layout will save costly debugging and rework. While TVS diodes are required to suppress the effects of direct charge injection that results from the ESD discharge, PCB design mainly impacts the effects due to the EM fields that are generated by the discharge current. This application note will provide PCB design guidelines for optimum ESD immunity.

**Circuit Loops**

Current is induced into any loop that encloses a changing magnetic flux. The magnitude of the current will be proportional to the size of the loop. Larger loops enclose more flux and thus higher currents are induced in the circuit. Therefore it is important to minimize loop areas. Some guidelines for minimizing loops areas are:

- One of the most common sources of loop areas are those formed by power and ground traces as shown in Figure 1. Whenever possible, multilayer PCBs with power and ground planes should be utilized. Multilayer boards not only minimize the loop area between power and ground, but also mitigate the effects of high frequency EMI fields that are produced by the ESD pulse.
- If a multilayer board is not feasible, then multiple power and ground traces should be connected in a grid pattern as shown in Figure 2. The grid emulates power and ground planes. Vias are used to connect traces on each layer. Connections should be made every 6cm in each direction.

- As a minimum alternative to power and ground grids or multilayer boards, keep power and ground traces close together (Figure 3).
- Another method for reducing loop area and induced currents is to minimize parallel paths between interconnected devices (Figure 4).
- Guard traces may be used in situations where a long (> 30cm) interconnected signal trace cannot be avoided (Figure 5). An even better solution is to place a ground plane opposite the signal line. The signal line should be within 13 mm of the guard trace or ground plane.
- Transpose long sections (> 30cm) of signal or power lines of very sensitive components with their ground line as shown in Figure 6. The lines should be transposed at regular intervals from top to bottom or left to right.

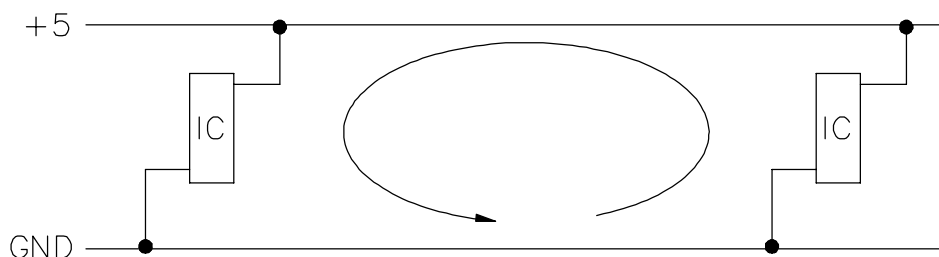
**Line Lengths**

Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced.

- Minimize interconnecting line lengths by placing devices with the most interconnects as close together as possible.

**Ground Charge Injection**

A direct ESD discharge into the ground plane can cause damage to sensitive circuits. One or more high



**Figure 1 - Power & Ground PCB Loop**

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frequency bypass capacitors along with a TVS diode should be placed between the power and ground of vulnerable components. The bypass capacitors serve to reduce charge injection and thus the voltage differential between power and ground. The TVS diverts induced currents and maintains the voltage differential at the level of the clamping voltage of the TVS. The TVS and capacitors should be placed as close as possible to the protected IC (Figure 7). Make sure TVS path length to ground & capacitor lead lengths are minimized to reduce the effects of parasitic inductance (described below).

Connectors should attach to the PCB by means of a copper land. Ideally, the land should be separate from the PCB ground plane and attached to the chassis via a short strap.

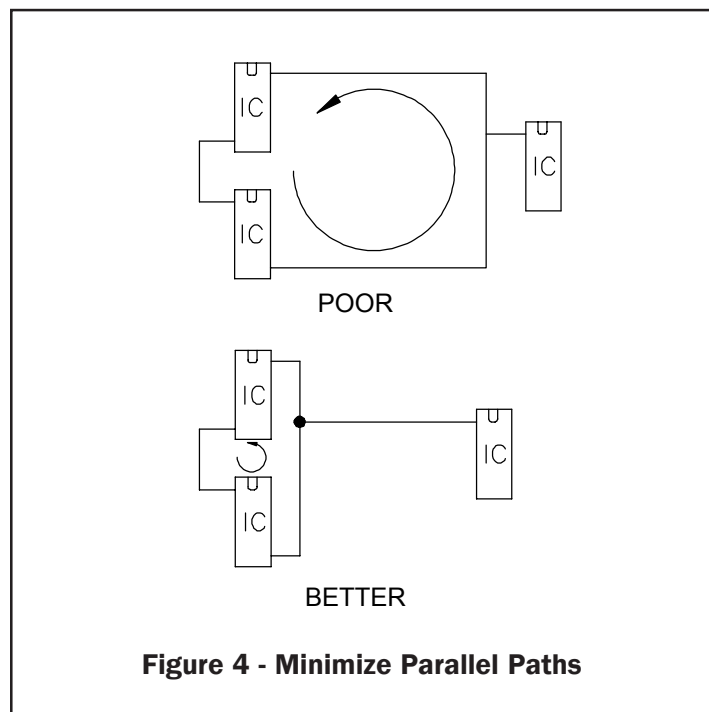
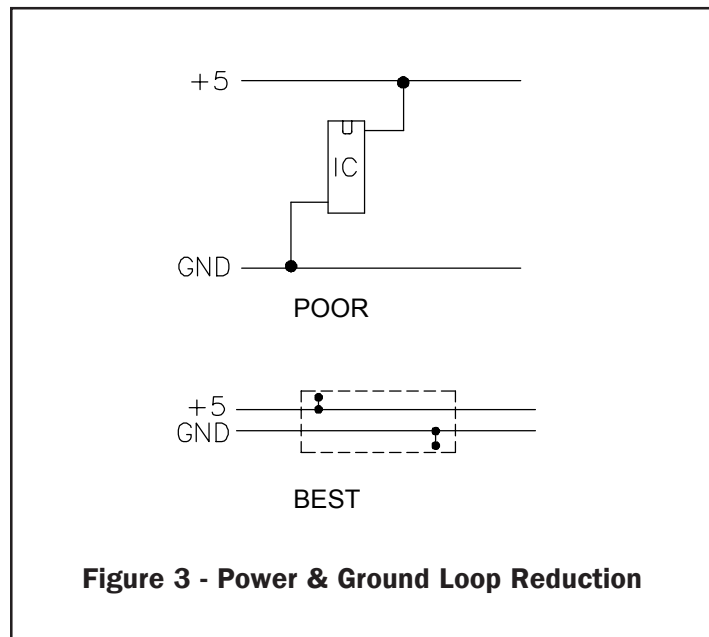
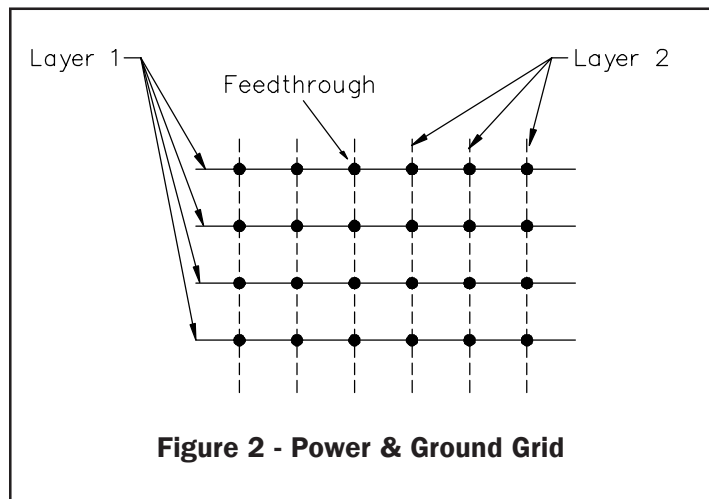
**Miscellaneous Guidelines**

- Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
- Fill unused portions of the PCB with ground plane.
- Separate chassis ground traces from components and signal traces by at least 4mm.
- Keep the chassis ground trace length-to-width ratio <5:1 to minimize inductance.
- Protect all external connections with TVS diodes.

**Parasitic Inductance in the Protection Circuit**

Parasitic inductance in the path of the TVS diode can result in severe voltage overshoot during an ESD event. Significant overshoot may still exceed the damage threshold of the protected IC despite the use of TVS diodes. Recall that the voltage developed across an inductive load is proportional to the time

rate of change in current flow ( $V_L = L di/dt$ ). The total voltage seen by the protected circuit will be the sum of clamping voltage of the TVS diode and the voltage due to parasitic inductance ( $V_T = V_C + V_L$ ). An ESD induced transient reaches a peak in less than 1ns (per IEC 61000-4-2). Assuming a trace inductance of 20nH per inch and a quarter inch trace, the voltage overshoot will be 50 volts for a 10A pulse. The primary rule of thumb is to minimize the effects of parasitic inductance by making the shunt paths as short as possible.



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All inductive paths must be considered including the ground return path, the path between the TVS and the protected line, and the path from the connector to the TVS device. Protected signal lines should be routed directly to the TVS diode. Ground connections should be made directly to the ground plane. If no ground plane is present, the ground return trace must be kept as short as possible. The distance between the ground connection of the TVS diode and the ground connection of the protected circuit should also be minimized to reduce parasitic inductance in the ground plane. Finally, The TVS device should be placed as close to the connector as possible to reduce transient coupling into nearby traces. The secondary effects of radiated emissions can cause upset to other areas of the board even if there is no direct path to the connector.

### References:

- Boxleitner, Warren, *“Electrostatic Discharge and Electronic Equipment,”* IEEE Press, 1989.
- Mardiguian, Michel, *“Electrostatic Discharge, Understand, Simulate and Fix ESD problems,”* Interference Control technologies, 1992.
- Russell, Bill, *“Power Protection is Critical For Today’s Shrinking System Designs,”* Wireless Systems Design, February 1999.
- Standler, Ronald B., *“Protection of Electronic Circuits from Overvoltages,”* John Wiley & Sons, 1989.

