Serial Routing and Distribution Product Configuration Loading Procedure

Application Note

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
8	043735	—	October 2018	Updates to Introduction, Device Power-up Sequence, Host Initiated Device Reset, and Configuration File.
7	043518	—	September 2018	Updates to Introduction, Device Power-up Sequence, Host Initiated Device Reset, and Configuration File.
6	037666	—	July 2017	Table 1 register values changed, and note added.
5	037358	—	June 2017	Added Device Power-up Sequence and Host Initiated Device Reset.
4	034403	—	November 2016	Minor update to Introduction regarding wait time.
3	034149	—	November 2016	Updated Introduction.
2	030308	—	March 2016	Minor updates to steps 7 and 8 in Appendix 1.
1	029877	—	March 2016	Minor updates to Appendix 1.
0	029404	—	January 2016	New document.

1. Introduction

This application note describes the procedure for loading a configuration into a Semtech SDI device. The example assumes that all devices in the group are identical, are using the same $\overline{CS}$ (chip select), and describes the use of broadcast mode to simultaneously configure all devices.

To confirm if a configuration file is required, complete one of the following two steps:

1. Read the Data Code from the top of the device package, and compare it to the values in Table 1. The location of the date code for each SRD device can be seen in Figure 1.
2. Perform a GSPI read from Register 0x0001 and compare it to the values in Table 1.

Note: If you have a Date Code or Device ID that is not present in Table 1, please contact your local Semtech FAE for support.

Table 1: SRD Identification Chart

Product	Device ID	Valid Date Codes	Required Configuration	Configuration Load Verification Register Address	Configuration Load Verification Register Value
	Read address 0x0001(15:0)*				
	Hex				
GS12150	7640 or 7648	1813*, ≥ 1826	GS12XXX_Config_5_E_0_1	0x81	0x0545
				0x82	0x0001
GS12142	6E44 or 6E4C	1813, ≥ 1826	GS12XXX_Config_5_E_0_1	0x81	0x0545
				0x82	0x0001
GS12182	5044 or 504C	1813, ≥ 1826	GS12XXX_Config_5_E_0_1	0x81	0x0545
				0x82	0x0001
GS12241	6E30 or 6E38	≥1729	Not Required	0x81	N/A
				0x82	N/A
GS12281	5030 or 5038	≥ 1730	Not Required	0x81	N/A
				0x82	N/A
GS12090	6AB0	≥ 1726	Not Required	0x81	N/A
				0x82	N/A
GS12081	5032 or 503A	≥ 1730	Not Required	0x81	N/A
				0x82	N/A
GS3241	6E31 or 6E39	≥ 1730	Not Required	0x81	N/A
				0x82	N/A
GS3281	5031 or 5039	≥1730	Not Required	0x81	N/A
				0x82	N/A
GS3590	6AB1	≥1730	Not Required	0x81	N/A
				0x82	N/A
GS12150	7620 or 7628	1738, 1750, 1813*	GS12182_x50_Config_4_T_0_27	0x81	0x0454
				0x82	0x001B
GS12142	6E24 or 6E2C	1745, 1814	GS12142_Config_4_C_0_11	0x81	0x0443
				0x82	0x000B

Table 1: SRD Identification Chart (Continued)

Product	Device ID Read address 0x0001(15:0)* Hex	Valid Date Codes	Required Configuration	Configuration Load Verification Register Address	Configuration Load Verification Register Value
GS12182	5024 or 502C	1740, 1814	GS12182_x50_Config_4_T_0_27	0x81	0x0454
				0x82	0x001B
GS12241	6E20 or 6E28	≥ 1710 to ≤ 1728	GS122XX_Config_4_S_0_26	0x81	0x0453
				0x82	0x001A
GS12281	5020 or 5028	≥ 1710 to ≤ 1729	GS122XX_Config_4_S_0_26	0x81	0x0453
				0x82	0x001A
GS12090	6AA0	≥ 1641 to ≤ 1725	GS122XX_Config_3_Z_4_39	0x81	0x035A
				0x82	0x0427
GS3590	6AA1	≥ 1721 to ≤ 1729	GS122XX_Config_3_Z_4_39	0x81	0x035A
				0x82	0x0427

Note:

- * If using a GS12150 that has a date code of 1813 and the assembly lot number (as shown in Figure 1) is 1626E3 or 2582E3, the required configuration is "GS12182_x50_Config_4_T_0_27". If the assembly lot number reads anything other than these values, the required configuration is GS12XXX_Config_5_E_0_1.

Figure 1: Date Code Identification

If the design has a mix of devices requiring different configurations, careful consideration is needed to minimize configuration time. The first option is to use a separate $\overline{CS}$ for each group of parts that requires the same configuration. A second, equally acceptable, option is to configure the unit addresses of each device first, and then write the device configuration independently. While this second option is perfectly acceptable, the configuration loading time will increase proportionally with the number of devices.

In all implementations, the host system must wait at least 5.11ms after power up before loading the configuration into the target devices. There is no upper time limit to loading the configuration settings, however the target devices will not perform as outlined in the data sheet specifications until the settings are loaded. After loading the configuration, the host must wait an additional 5ms before writing any additional register settings.

The device is held in reset during configuration loading, so the signal path through the device will be interrupted during this time.

Refer to the to the individual device datasheets for GSPI implementation details and Host Interface Register Map for register description details.

2. Device Power-up Sequence

The power supply should be designed so all rails reach a minimum of 90% of the specified rail voltage at the same time. If this is not possible, ensure VCC_DDI / VCC_SDI reaches this level first. There is no minimum time required between other power supply rails.

2.1 Device Initialization Sequence

The steps below must be followed after the device is powered on, or after a device reset.

Additional detail on each step can be found in the timing diagram shown in Figure 2. Where applicable, steps listed below are indicated by the letters A through G in parentheses. These letters highlight the location of the step in Figure 2.

1. Power on or reset the device.
   Note: For more information about preforming a device reset through the host interface see Section 3.
2. Wait 5.11ms or longer. (A to B)
3. If multiple devices operating in either Loop-Through or Bus-Through configuration share the same chip select line, configure GSPI unit addresses. Information on this can be found in the section titled "Setting a Device Unit Address" of the target device Data Sheet.
   Note: Optionally, this step may be skipped if all devices using the same chip select line are identical.
4. Read Device ID from register 0x0001, and compare to the values in the Device ID column of Table 1 to determine if configuration loading is required.
5. Load the specified configuration (if applicable) by writing the data values to each address specified in the Semtech-provided file. (C)
   Note: If multiple devices operating in either Loop-Through or Bus-Through configuration share the same chip select line, and have the same required configuration indicated in Table 1, set the BCAST ALL bit in the GSPI COMMAND 1 word to broadcast the configuration to all devices using the active chip select line.
6. Wait 5ms or longer. (D)
7. Host sets **EYE_MON_INT_CFG_3** (register address 0x57) to 0x8006.
   Note: This step is only required for GS12241, GS12281, GS12090, and GS3590.
8. Confirm the configuration has been successfully loaded by comparing the values in registers 0x81 and 0x82 to those shown in the "Configuration Load Verification Register Value" column of Table 1.
9. If there are multiple devices operating in either Loop-Through or Bus-Through configuration sharing the same chip select line, configure unique GSPI unit addresses as described in the section titled "Setting a Device Unit Address" of the target device, if not already done in Step 3. (E)
10. Normal operation begins. (E)

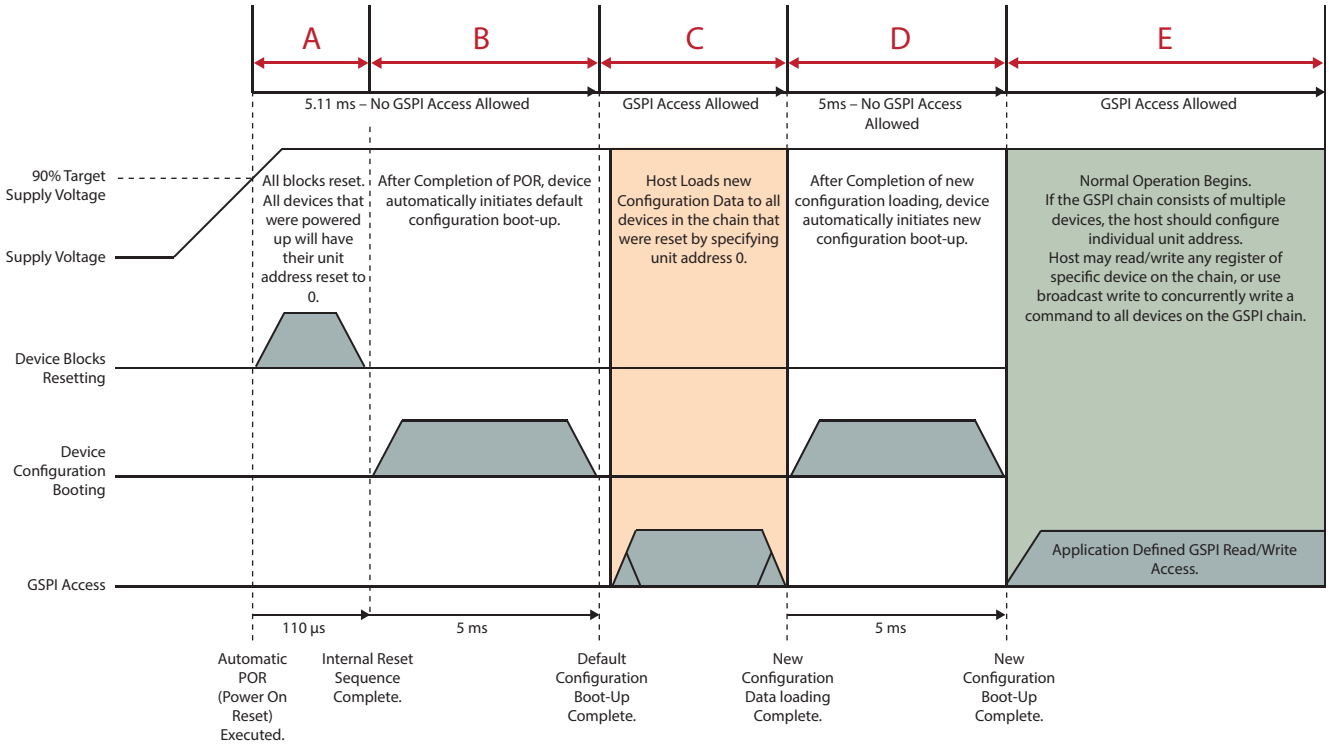

Figure 2: Power-up Sequence (Including External Configuration Loading)

3. Host Initiated Device Reset

The Serial Routing and Distribution devices include a reset function accessible via the device's host interface, which reverts all internal logic and register values to their default states.

The device can be reset with a single write of AD00 to the **RESET_CONTROL** bits of the **CONTROL_RESET** register, which will assert and de-assert the device reset within the duration of the GSPI write access Data Word.

The device can be placed and held in reset by writing AA00 to the **RESET_CONTROL** bits of the **CONTROL_RESET** register. Subsequent writes of DD00 to the **RESET_CONTROL** bits will de-assert device reset.

The current state of user-initiated device reset can be read from the **RESET_CONTROL** bits of **CONTROL_RESET** register.

While in reset, host interface accesses to any other register is prevented and all logic and configuration registers will be in reset state. While in reset, serial output signal behaviour is undefined. The digital logic and registers within the device will exit the reset state 5.11ms after device reset is de-asserted.

Please see 2.1 Device Initialization Sequence for the required steps to initialize the device after a host initiated reset has been performed.

4. Configuration File

The configuration is provided by Semtech as a text file with the following naming convention:

'GS12XXX_Config_z_E_z_z.txt', where 'z_E_z_z' is the version number. For example, version 5_E_0_1 of the file will be named: GS12XXX_Config_5_E_0_1.txt.

After the configuration is loaded, the host should read the addresses listed under the "**Configuration Load Verification Register Address**" column in Table 1 and confirm that they match the values listed under column "**Configuration Load Verification Register Value**" to verify the version number and confirm successful loading.

The file itself is formatted as follows:

The first line of the file contains the column descriptions for the three columns of the file.

The three columns are space delimited and of fixed width of 5 characters wide. The first column is the instruction number, the second column is the target register address and the third column is the data to be written to that register address.

For example, the first and last few instructions of the GS12XXX_Config_5_E_0_1 configuration are:

Word	Address	Data
1	0002	0005
2	0002	0001
3	6390	90C9
...	...	...
64	63CD	0100
65	010E	6390
66	0002	0000

All of the data from each line must be written to the associated addresses before the device can begin normal operation.

In this example, all but the first two and last two data writes are sequentially addressed. The loading speed of the configuration file can be increased by using the device auto-increment method for sequential loading of the sequentially addressed data. Before using the auto-increment write feature, open the required configuration file being used, and check the first and last few lines of the file to see where to start and stop sequential addressing for the specific configuration file in use.

Appendix 1

The following is an example of byte-wise instructions for loading the GS121XX_Config_2_E_0_9.txt configuration file to all the devices in the GSPI chain and for setting individual Unit Addresses of each device.

All devices power-up with a default Unit Address 0. With the intent to simultaneously configure all the devices on a single GSPI chain, writing the instructions to Unit Address 0 will broadcast the instruction to all the devices. This means that the broadcast bit (B'CAST ALL) does not need to be set.

In this example, the host performs the following steps:

- Loads the configuration file:
  1. Single write data = 0x0005, to address 0x0002.
  2. Single write data = 0x0001, to address 0x0002.
  3. Sequential data write using Auto-Increment starting at address 0x6390, where the first data word is 0x90C9 and the ending address being 0x63CD, with the last data word being 0x0100.
  4. Single write data = 0x6390, to address 0x010E.
  5. Single write data = 0x0000, to address 0x0002.
- Assigns Unit Addresses to all the devices in the GSPI chain:
  1. Repeat instruction a) and b) for every device in the GSPI chain.

     a) Single write data = 0x4000, to address 0x0 specifying Unit Address 0.

     b) Single write data = 0xzz, to address 0x0 specifying Unit Address 0, where zz are the desired individual Unit Addresses. E.g. zz = 1, 2, 3, 4, 5, 6, 7, 8 for eight devices sequentially named.
- Verify the load by reading the configuration file version number from the register addresses listed under the "**Configuration Load Verification Register Address**" column in Table 1, and confirm that they read back the values listed under column "**Configuration Load Verification Register Value**." This can be done one device at a time using single read or Auto-Increment read.

Byte-wise Configuration example for GS122XX_Config_5_E_0_1

The following is the bit level command instructions to load the configuration and initialize Unit Addressing.

1st Instruction write Extentended Addressing Unit Address = 0

Address	0x0002
Data	0x0005

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address								Upper 7 bits of Reg Add								Lower 16 bits of Register Address											
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Hex	2				0				0				0				0				0				0				2			

Byte Number	Byte 5								Byte 6							
Type	Read/Write Data1															
Description	Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
Hex	0				0				0				5			

2nd Instruction write Extentended Addressing Unit Address = 0

Address	0x0002
Data	0x0001

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address								Upper 7 bits of Reg Add								Lower 16 bits of Register Address											
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Hex	2				0				0				0				0				0				0				2			

Byte Number	Byte 5								Byte 6							
Type	Read/Write Data1															
Description	Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Hex	0				0				0				1			

- After the first two instructions, the next 61 instructions are sequentially addressed. Depending on the buffer size of host GSPI driver implementation, the configuration file loading speed can be greatly increased by using Auto-Increment mode.

Instruction 3-64 write Extentended Addressing Auto Increment = 1 Unit Address = 0

Address	From	To
	0x6390	0x63CD
Data	From	To
	0x90C9	0x0100

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address								Upper 7 bits of Reg Add								Lower 16 bits of Register Address											
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1	0	0	0	0
Hex	3				0				0				0				6				3				9				0			

Byte Number	Byte 5								Byte 6								Byte 7								Byte 8								...								...			
Type	Read/Write Data1																Read/Write Data2 in Auto Increment Mode																Read/Write ... in Auto Increment Mode											
Description	Data																Data																Data											
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	1	0	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0																		
Hex	9				0				C				9				0				4				E				0				...				...				...			

- After the sequential portion of the configuration has been loaded, the following 2 additional writes are required.

65th Instruction write Extentended Addressing Unit Address = 0

Address	0x010E
Data	0x6390

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0
Hex	2				0				0				0				0				1				0				E			

Byte Number	Byte 5								Byte 6							
Type	Read/Write Data1															
Description	Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	1	1	0	0	0	1	1	1	0	0	1	0	0	0	0
Hex	6				3				9				0			

66th Instruction write Extentended Addressing Unit Address = 0

Address	0x0002
Data	0x0000

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Hex	2				0				0				0				0				0				0				2			

Byte Number	Byte 5								Byte 6							
Type	Read/Write Data1															
Description	Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Hex	0				0				0				0			

- After the configuration file is loaded to all the devices on the single GSPI chain, the last step is to assign a unique Unit Address to each device on the chain. Repeat Instructions 1 and 2 below for each device in the chain and assign a unique Unit Address 'zz'.

1st Instruction
write
Extentended Addressing
Unit Address = 0

Address	0x0
Data	0x4000

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Hex	2				0				0				0				0				0				0				0			

Byte Number	Byte 5								Byte 6							
Type	Read/Write Data1															
Description	Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Hex	4				0				0				0			

2nd Instruction
write
Extentended Addressing
Unit Address = 0

Address	0x0
Data	0xzz
assign unit address 'zz' to last device in the chain	

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Hex	2				0				0				0				0				0				0				0			

Byte Number	Byte 5								Byte 6							
Type	Read/Write Data1															
Description	Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	0	0	0	z	z	z	z	z	z	z	z
Hex	0				0				z				z			

- After this step, all the devices in the chain should be properly configured and have unique Unit Addresses. The device is ready for normal operation and the first operation should be to verify the configuration file was loaded properly by reading the register addresses listed under "**Configuration Load Verification Register Address**" column in Table 1, and confirming that they read back the values listed under column "**Configuration Load Verification Register Value**."

1st Instruction read Extentended Addressing Unit Address = z

Address	0x0081
Data	0x0545

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	1	0	1	0	z	z	z	z	z	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
Hex	A				z				z				0				0				0				8				1			

69 is the asc character for E

Byte Number	Byte 5								Byte 6							
Type	Read Data1															
Description	Requested Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	1
Hex	0				5				4				5			

2nd Instruction read Extentended Addressing Unit Address = z

Address	0x0082
Data	0x0001

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	1	0	1	0	z	z	z	z	z	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Hex	A				z				z				0				0				0				8				2			

Byte Number	Byte 5								Byte 6							
Type	Read Data1															
Description	Requested Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Hex	0				0				0				1			

- Or using Auto-Increment mode

Instruction 1-2 read Extentended Addressing Auto Increment = 1 Unit Address = z

Address	From	To
	0x0081	0x0082
Data	From	To
	0x0545	0x0001

Byte Number	Byte 1								Byte 2								Byte 3								Byte 4							
Type	Command 1																Command 2															
Description	R/W	BCS	EM	AI	Unit Address				Upper 7 bits of Reg Add								Lower 16 bits of Register Address															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	1	0	1	1	z	z	z	z	z	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
Hex	B				z				z				0				0				0				8				1			

Byte Number	Byte 5								Byte 6								Byte 7								Byte 8							
Type	Read Data1																Read Data2 in Auto Increment Mode															
Description	Requested Data																Data															
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bin	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Hex	0				5				4				5				0				0				0				1			

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com