

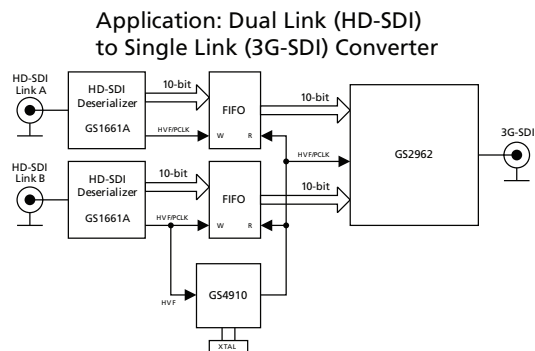


GS1661A HD, SD SDI Receiver, with Integrated Adaptive Cable Equalizer

Key Features

- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 292M, SMPTE 259M-C and DVB-ASI
- Integrated adaptive cable equalizer
- Typical equalized length of Belden 1694A cable:
 - ♦ 250m at 1.485Gb/s
 - ♦ 480m at 270Mb/s
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked output
- Ancillary data extraction
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 460mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications



Description

The GS1661A is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE 292M and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS1661A integrates Gennum's next-generation state-of-the-art adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The Serial Digital Output can be connected to an external Cable Driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS1661A performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS1661A also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE 352M packet detection and decoding. All of the processing features are optional, and may be enabled or disabled via the Host Interface.

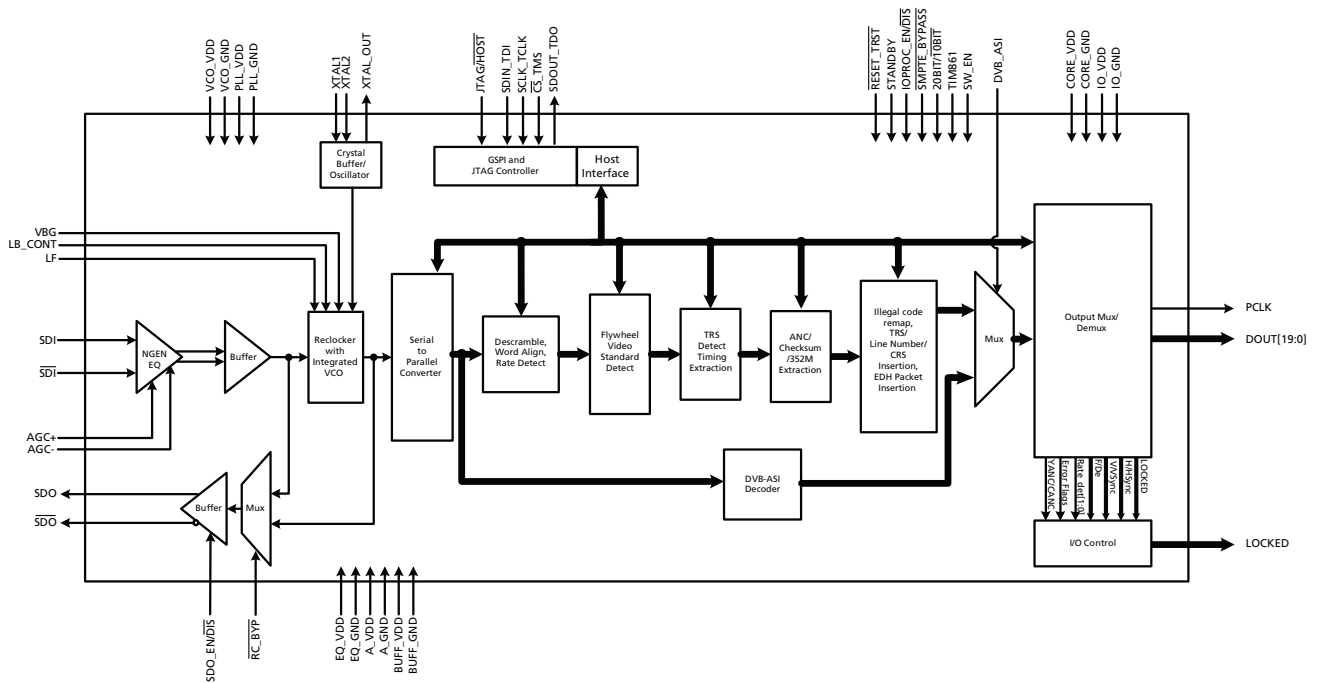
In DVB-ASI mode, 8b/10b decoding is applied to the received data stream.

In Data-Through mode, all forms of SMPTE and DVB-ASI decoding are disabled, and the device can be used as a simple serial to parallel converter.

The device can also be placed in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static. Placing the Receiver in Standby mode will automatically place the integrated equalizer in power down mode as well.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for HD and SD video rates. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (HD 10-bit multiplexed modes), 74.25 or 74.25/1.001MHz (for HD 20-bit mode), 27MHz (for SD 10-bit mode) and 13.5MHz (for SD 20-bit mode).

Functional Block Diagram



GS1661A Functional Block Diagram

Pin Out

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_VDD	RSV	VCO_GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_VDD	PLL_VDD	STAT4	STAT5	RESET_TRST	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SW_EN	JTAG_HOST	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SDOUT_TDO	SDIN_TDI	DOUT10	DOUT11
F	AGC+	RSV	A_GND	PLL_GND	CORE_GND	CORE_VDD	$\overline{\text{CS}}$ _TMS	SCLK_TCK	DOUT8	DOUT9
G	AGC-	A_GND	$\overline{\text{RC}}$ _BYP	CORE_GND	CORE_GND	CORE_VDD	$\overline{\text{SMPTE}}$ _BYPASS	DVB_ASI	IO_GND	IO_VDD
H	BUFF_VDD	BUFF_GND	CORE_GND	RSV	TIM_861	XTAL_OUT	20bit/10bit	IOPROC_EN/DIS	DOUT6	DOUT7
J	SDO	SDO_EN/DIS	RSV	RSV	RSV	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	RSV	RSV	RSV	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

GS1661A Pin Out

The following table shows the pin difference between the GS1660A and the GS1661A:

Pin Number	GS1660A	GS1661A	Functional Description of the GS1661A Pins
E1	SDI_VDD	EQ_VDD	POWER pin for the EQ.
E2	SDI_GND	EQ_GND	GND pin for the EQ.
F1	TERM	AGC+	Attach the AGC capacitor between this pin and AGC-.
G1	RSV	AGC-	Attach the AGC capacitor between this pin and AGC+.
G2	RSV	A_GND	Level adjust for the Equalizer.
G4	RSV	CORE_GND	GND connection – digital logic.
H3	RSV	CORE_GND	GND connection – digital logic.

DOCUMENT IDENTIFICATION
PRODUCT BRIEF

The product is in a development phase and specifications are subject to change without notice. Gennum reserves the right to remove the product at any time. Listing the product does not constitute an offer for sale.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A
STATIC-FREE WORKSTATION

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