



Application Note

HD/SD Transmitter and Receiver Designs with Migration Path to 3G

Preface

This Application Note focuses on the differences between Gennum's HD/SD transmitter-receiver set and Gennum's 3G/HD/SD transmitter-receiver set. It provides information on the hardware and firmware requirements for designing a HD/SD system using Gennum's HD/SD parts with the option of upgrading to 3G, effectively replacing the GS1671 and the GS1672 with the GS2971 and the GS2972.

Overview

The GS1672 and the GS2972 are pin-to-pin compatible and functionally similar. The one difference between them is that the GS2972 supports 3Gb/s SDI video (SMPTE 424M). Due to the additional data rate supported by the GS2972, there is a set of bits in the GS2972's registers unavailable in the GS1672. Furthermore, there is a difference in the function of one pin, which is used to set the 3G data rate for the GS2972. That pin should be grounded on the GS1672.

The GS1671 and the GS2971 are pin-to-pin compatible, with same functionality for all of the pins. The only difference is a set of bits in the GS2971 registers unavailable in the GS1671. These registers are for 3G applications.

Transmitters

Pin Comparison

Pin	GS1672 Pin Name	GS1672 Pin Function	GS2972 Pin Name	GS2972 Pin Function
E3	RATE_SEL	Used to set the data rate: 0 - HD 1 - SD	RATE_SELO	Used to set the data rate: 0 - depends on RATE_SEL1 1 - SD
E4	RSV	Reserved	RATE_SEL1	If RATE_SELO - 0: 0 - HD 1 - 3G

For the GS1672, pin E4 is a reserved pin which should be tied to ground. In order to make the system compatible with the GS2972, designers can connect this pin to a pin on the FPGA or microcontroller (which controls the GS1672), and that pin should be set to 0 when the GS1672 is implemented. Alternatively, this pin can be pulled LOW by using a

resistor and connected to the FPGA (microcontroller). In this case, the pin on the FPGA (microcontroller) will be programmed to a high-impedance state.

Register Comparison

Due to the additional data rates supported by the GS2972, there are extended definitions for bit functions compared to the GS1672. Furthermore, there are some bits in the video core registers that have additional functions for the GS2972 (these registers are for 3G applications only).

Address	Bit	GS1672 Function	GS2972 Bit Name	GS2972 Bit Function
000h	13	Reserved	AUDIO_LEVELB_STREAM_2_1B	HIGH - embeds audio on the DS2 of a 3G Level B signal. LOW - embeds audio on the DS1 of a 3G Level B signal.
000h	9	Reserved	CONV_372	HIGH - disables Level A-B conversion. LOW - enables Level A-B conversion.
20Dh	8	Reserved	LEVEL_B	HIGH indicates that Level B has been detected.

Receivers

Pin Comparison

The GS1671 and the GS2971 are completely pin-to-pin compatible.

Register Comparison

Due to the additional data rates supported by the GS2971, there are extended definitions for bit functions compared to the GS1671. Furthermore, there are some bits in the video core registers that have additional functions for the GS2971 (these are for 3G applications only).

Address	Bit	GS1671 Function	GS2971 Bit Name	GS2971 Bit Function
001h	12	Reserved	TRS_WORD_REMAP_DS2_DISABLE	Disables the 8-bit TRS word remapping in Data Stream 2 (3G Level B only)
001h	10	Reserved	REGEN_352M_MASK	Disables regeneration of the SMPTE 352M packet for 3G Level B data
001h	9	Reserved	DS_SWAP_3G	Swaps Data Stream 1 (DS1) and Data Stream 2 (DS2) at the output in 3G mode
001h	8	Reserved	LEVEL_B2A_CONV_DISABLE_MASK	Disable the conversion of a 3G Level B input to a 3G Level A format
014h	15:0	Reserved	ANC_TYPE1_DS2	Programmable DID/SDID
015h	15:0	Reserved	ANC_TYPE2_DS2	Programmable DID/SDID

Address	Bit	GS1671 Function	GS2971 Bit Name	GS2971 Bit Function
016h	15:0	Reserved	ANC_TYPE3_DS2	Programmable DID/SDID
017h	15:0	Reserved	ANC_TYPE4_DS2	Programmable DID/SDID
018h	15:0	Reserved	ANC_TYPE5_DS2	Programmable DID/SDID
01Bh	15:0	Reserved	VIDEO_FORMAT_2_DS2 VIDEO_FORMAT_1_DS2	SMPTE 352M embedded packet bytes 1 and 2
01Ch	15:0	Reserved	VIDEO_FORMAT_4_DS2 VIDEO_FORMAT_3_DS2	SMPTE 352M embedded packet bytes 3 and 4
01Dh	15:0	Reserved	VIDEO_FORMAT_2_INS VIDEO_FORMAT_1_INS	SMPTE 352M packet - bytes 1 and 2 to be embedded
01Eh	15:0	Reserved	VIDEO_FORMAT_4_INS VIDEO_FORMAT_3_INS	SMPTE 352M packet - bytes 3 and 4 to be embedded
023h	4	Reserved	V_LOCK_DS2	Indicates a lock to vertical timing (3G Level B Data Stream 2 only)
023h	3	Reserved	H_LOCK_DS2	Indicates a lock to horizontal timing (3G Level B Data Stream 2 only)
038h	6:0	Reserved	ERROR_MASK_2	Error mask for global error vector (3G Level B Data Stream 2 only)
06Ch	5	Reserved	DEL_LINE_CLK_SEL	In-phase (0) or quadrature (1) clocks for DDR mode

References

- GS1671 Data Sheet (Doc ID 53737)
- GS1672 Data Sheet (Doc ID 53623)
- GS2971 Data Sheet (Doc ID 45898)
- GS2972 Data Sheet (Doc ID 47479)
- GS2970 Design Guide (Doc ID 48558)
- GS2972 Design Guide (Doc ID 48581)

Revision History

Version	ECR	Date	Changes and/or Modifications
1	153575	January 2010	Correction to Receiver/Transmitter Heading Introductions.
0	153338	January 2010	New document.

DOCUMENT IDENTIFICATION

APPLICATION NOTE

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