GS2970/GS2971 Errata

Fill out a technical support request at http://www.gennum.com/support/tech_inquiry.php to receive FPGA work-around code where available as described below:

1. Audio channels 3~8 output misaligned to WCLK for SD formats

Devices Affected: GS2970 & GS2971.

Workaround Available: Yes. The workaround can be implemented in an FPGA. The workaround requires FPGA logic resources, connectivity to affected products (GSPI interface and other signals).

Impact: If using serial audio and the condition occurs (CH3-8 are not aligned to the WCLK), the output audio will be corrupt. AES/EBU has embedded clock information, so the condition can still happen, but the output audio will not be corrupted.

Summary: Under certain conditions, audio channels 3-8 get misaligned with the WCLK, hence leading to corrupted audio for applications using serial audio.

Detailed Description:

This is a problem with I^2S and serial audio output modes by corrupting the audio data only, and does not corrupt AES/EBU audio data in AES mode.

The audio at AOUT1/2 will always be aligned to WCLK output.

Audio outputs AOUT3/4, AOUT5/6 and AOUT7/8 may be misaligned, as shown in Figure 1-1:

Figure 1-1: Audio Channel Misalignment

The problem occurs randomly after the device has locked or re-locked to the video source. Sometimes all channels will be aligned to WCLK and sometimes not.

This problem occurs due to an internal audio word clock offset for audio outputs 3 through 8 caused by misdetection of the audio 5-frame sequence. The device only has one WCLK output taken from the source of AOUT1/2. The system is unable to detect the misalignment of audio outputs 3 through 8 since their respective word clocks are not provided external to the device.

Since AOUT1/2 is always aligned to the WCLK output, the first two channels of audio from the selected primary audio group will always be aligned to WCLK. By default, audio channels 1 and 2 from embedded audio Group 1 (primary audio group) will always be aligned to WCLK. If embedded audio Group 2 is set as the primary audio group, audio channels 5 and 6 will always be aligned to WCLK. See Figure 1-2 below. The primary audio group is selected using the IDA[1:0] bits in register 400h.

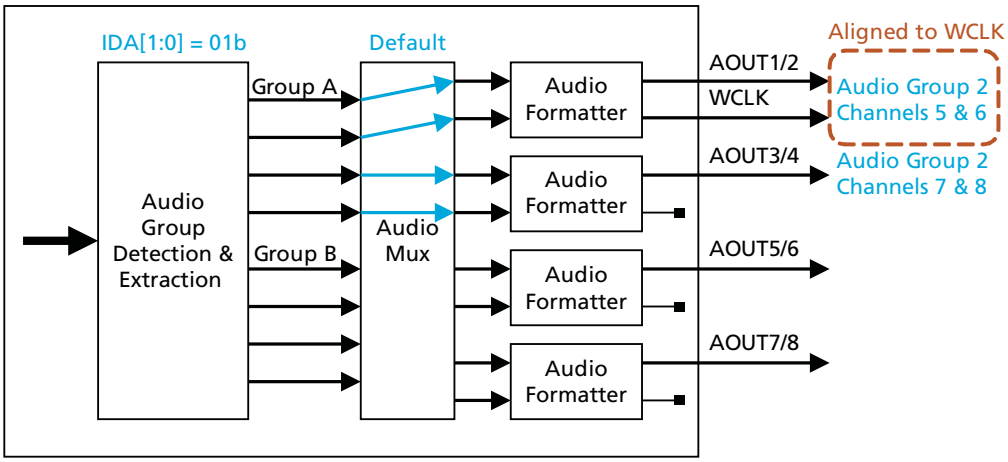

Figure 1-2: Audio Group 2 Selected as Primary Audio Group

Gennum will provide FPGA IP code as a workaround for this bug.

2. Audio channel offset within audio channel pair for SD formats

Devices Affected: GS2970 & GS2971.

Workaround Available: Currently, no workaround is available.

Impact: Audio is not corrupted.

Summary: Under certain conditions, one audio channel in a pair might get misaligned relative to the other channel within the pair.

Detailed Description:

This is a problem in I^2S mode, serial audio modes, as well as AES mode.

This problem will only occur when the device is de-embedding audio from an SD video source. The problem occurs randomly after the device has locked or re-locked to the video source (SDI input source is repeatedly plugged and un-plugged).

Within an audio channel pair, one of the channels (left or right for stereo) may be offset by one WCLK with respect to the samples original position. This is illustrated in Figure 2-1 below.

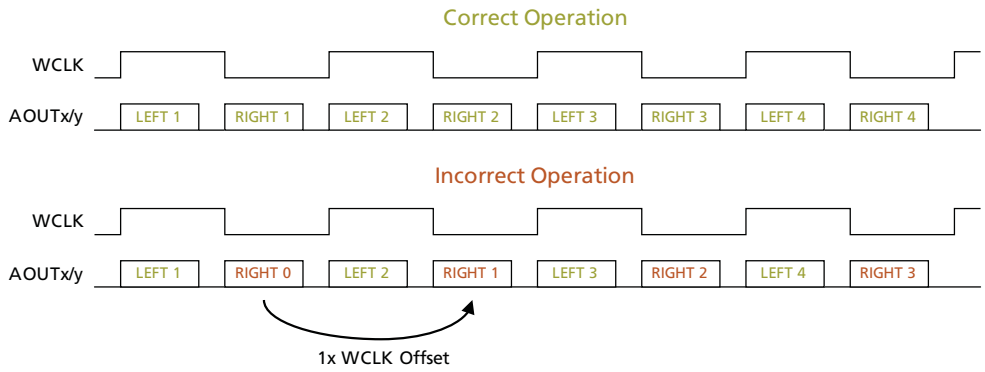

Figure 2-1: Audio Channel Offset

This offset can occur in any of the channel pair outputs, AOUT1/2, AOUT3/4, AOUT5/6 or AOUT7/8, and in any of the audio output modes, including AES. The offset can also occur with the first or second channel within an audio channel pair. The problem occurs randomly after the device has locked or re-locked to the video source.

Currently, no workaround is available for this issue.

3. Erroneous audio outputs when Audio Group removed from HD or 3G source

Devices Affected: GS2970 & GS2971.

Workaround Available: Yes. The workaround is a set of recommendations for action by equipment firmware, and small circuit implementation in FPGA.

Impact: Audio gets corrupted if condition occurs.

Summary: When there is no embedded audio in one of the groups, the device outputs invalid data on the channels within that audio group.

Detailed Description:

This is a problem in I^2S mode, serial audio modes, as well as AES mode.

This problem only affects the device when operating with HD or 3G formats.

When the device is de-embedding two audio groups from an HD or 3G source, if one or both of the embedded audio groups are no longer present in the input, the corresponding audio outputs (by default, AOUT1/2 and AOUT3/4 for Group 1 or AOUT5/6 and AOUT7/8 for Group 2) may sometimes output erroneous data.

In this scenario, the audio mute functions (via host interface register 200h for MUTE_ALL or register 205h for MUTEA/B) do not function, and erroneous data continues to be output, even when an output has been set to mute.

The user can check the audio group detect bits (ADPGx_DET, bits 4:1) in register 202h of the host interface to check when the audio group is no longer present. If one of the embedded audio groups is no longer present, the corresponding audio outputs should be ignored by the system. Since the workaround involves mostly polling the register above, there is no need for Gennum to provide any FPGA IP workaround for this bug.

The mute function works correctly when the device is extracting audio from both audio groups.

4. WCLK (and other audio clocks) output frequency variation when plugging and un-plugging SDI input

Devices Affected: GS2970 & GS2971.

Workaround Available: Yes. The workaround can be implemented in an FPGA. The workaround requires FPGA logic resources, connectivity to affected products (GSPI interface and other signals).

Impact: Audio gets corrupted if condition occurs. Recommend implementation of FPGA IP workaround.

Summary: Under certain conditions, WCLK can vary slightly from 48kHz (47kHz to 49kHz).

Detailed Description:

This is a problem in I^2S mode, serial audio modes, as well as AES mode.

This problem occurs for all SD, HD and 3G formats.

When the SDI input source is repeatedly plugged and un-plugged, the WCLK output timing may not always be correctly set to 48kHz. The variation occurs randomly, and can be between 47kHz and 49kHz. When this variation happens in WCLK, the variation is also observed in AMCLK and ACLK, since these two clocks are derived from the same clock generator base as the WCLK.

When the device unlocks and then re-locks to the SDI signal, the internal audio timing generator must be reset via the host interface. To reset the audio timing generator, write 0x004 into reserved register 05Eh to set the Audio Clock Gen bit 2, and then write 0x000 to address 05Eh to bring it back out of reset.

The system may monitor the locked status of the device via the LOCKED output signal (default STAT3 ball B6), or via the STD_LOCK bit 12 in host interface register 022h.

Gennum will provide a workaround for this bug in the form of FPGA IP and instructions on programming the GS2970/GS2971 registers as outlined above.

5. Video line number error flag stuck HIGH when HD/3G input format changes

Devices Affected: GS2960 & GS2961; GS2970 & GS2971

Workaround Available: Yes. The workaround is a set of recommendations for action by equipment firmware, and requires GSPI connectivity with the device.

Impact: Video is not impacted. This affects only the line number monitoring function.

Summary: The Line Number Error flag might be set HIGH, even though there are no line number errors.

Detailed Description:

This problem occurs when the HD or 3G input format changes (for example: when the input HD source changes between 1080i and 720p, or when the 3G source changes between 1080p60 and 1080p59.94).

When the HD/3G input format changes, the line number error flag may be set to denote a line number error (LNUM_ERR bit 2 in register 002h set HIGH). In this case, one of two things may have occurred:

1. The error flag is set HIGH, even though there is no line number error in the input source.
2. The error flag is set HIGH, the device is programmed to insert line numbers (enabled by default), and the device may have inserted incorrect video line numbers.

Even though the error flag register 002h is “clear on write”, writing all ones to this register will not clear the LNUM_ERR flag as expected.

There are two possible ways to clear the line number error flag:

1. Reset the device.
2. Toggle reserved bit 13 HIGH then LOW in register 000h.

If the system is not using the line number error reporting function, the system can mask this error flag by setting the ERROR_MASK bit 2 HIGH in register 037h.

If the system is not using the line number insertion function, the system can disable this permanently by setting the LNUM_INS_MASK bit 1 HIGH in register 000h.

6. Chroma channel ancillary data checksum error flag stuck HIGH when switching from HD/3G to SD formats or from HD/3G to HD/3G formats with no CANC data

Devices Affected: GS2960 & GS2961; GS2970 & GS2971.

Workaround Available: Yes. The workaround is a set of recommendations for action by equipment firmware, and requires GSPI connectivity with the device.

Impact: Video is not impacted. This affects only the CANC checksum monitoring function.

Summary: The CANC checksum error flag might be set HIGH after switching input formats, even though the flag might be irrelevant.

Detailed Description:

This problem occurs when switching from any HD/3G input format to any SD format. It also occurs when switching from any HD/3G input format to any HD/3G format with no ancillary data in the Chroma video data stream (CANC).

When the HD/3G input changes to SD or HD/3G input (with no CANC data), the Chroma channel checksum error flag may be set to denote a checksum error (CCS_ERR bit 6 in register 002h set HIGH). The error flag is set HIGH during the format switch and continues to be set HIGH because the flag is only cleared when new CANC data is present.

Even though the error flag register 002h is “clear on write”, writing all ones to this register will not clear the CCS_ERR flag as expected. The flag can be cleared by resetting the device.

Since the CCS_ERR error flag is not applicable in SD mode, the user can mask this bit when they switch to an SD format by setting the CCS_ERR bit 6 HIGH in the ERROR_MASK register 037h.

For HD/3G mode, the user can monitor the Chroma ancillary data via the C/2ANC signal on one of the STAT output pins. This pin is HIGH whenever ANC data is detected in the Chroma data stream, and LOW when no ANC data is detected. If this output stays LOW, there is no ancillary data in the Chroma stream and the CCS_ERR bit can be ignored by masking the CCS_ERR bit in the ERROR_MASK register 037h. If there is ancillary data present on the Chroma stream then the CCS_ERR flag that is stuck will be cleared once the next CANC data is detected by the device.

7. Luma channel ancillary data checksum error flag stuck HIGH when switching from SD/HD/3G to SD/HD/3G formats with no YANC data

Devices Affected: GS2960 & GS2961; GS2970 & GS2971.

Workaround Available: Yes. The workaround is a set of recommendations for action by equipment firmware, and requires GSPI connectivity with the device.

Impact: Video is not impacted. This affects only the YANC checksum monitoring function.

Summary: The YANC checksum error flag might be set HIGH after switching input formats, even though flag might be irrelevant.

Detailed Description:

This problem occurs when switching from any SD/HD/3G input format to any SD/HD/3G format with no ancillary data in the Luma video data stream (YANC). If YANC packets are present in the input video, this problem will not occur.

When the format change occurs, the Luma channel checksum error flag may be set to denote a checksum error (YCS_ERR bit 5 in register 002h set HIGH). The error flag is set HIGH during the format switch, and continues to be set HIGH because the flag is only cleared when new YANC data is present.

Even though the error flag register 002h is “clear on write”, writing all ones to this register will not clear the YCS_ERR flag as expected. The flag can be cleared by resetting the device.

The system can monitor the Luma ancillary data status via the Y/1ANC signal on one of the STAT output pins (default STAT4 ball C5). This output is HIGH whenever ANC data is detected in the Luma data stream, and LOW when no ancillary data is detected. If this bit stays LOW, there is no YANC data in the Luma stream and the YCS_ERR bit can be ignored by masking the YCS_ERR bit in the ERROR_MASK register 037h. If there is ancillary data present on the Luma stream then the YCS_ERR flag that is stuck will be cleared once the next YANC data is detected by the device.

Revision History

Version	ECR	Date	Changes
3	153147	November 2009	Updates.
2	152588	September 2009	Updates.
1	152489	August 2009	Updates.
0	152266	July 2009	New document.

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GENNUM CORPORATE HEADQUARTERS
4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
Phone: +1 (905) 632-2996
E-mail: corporate@gennum.com
Fax: +1 (905) 632-2055
www.gennum.com

OTTAWA
232 Herzberg Road, Suite 101
Kanata, Ontario K2K 2A1
Canada
Phone: +1 (613) 270-0458
Fax: +1 (613) 270-0429

CALGARY
3553 - 31st St. N.W., Suite 210
Calgary, Alberta T2L 2K7
Canada
Phone: +1 (403) 284-2672

UNITED KINGDOM
North Building, Walden Court
Parsonage Lane,
Bishop's Stortford Hertfordshire, CM23 5DB
United Kingdom
Phone: +44 1279 714170
Fax: +44 1279 714171

INDIA
#208(A), Nirmala Plaza,
Airport Road, Forest Park Square
Bhubaneswar 751009
India
Phone: +91 (674) 653-4815
Fax: +91 (674) 259-5733

SNOWBUSH IP - A DIVISION OF GENNUM
439 University Ave. Suite 1700
Toronto, Ontario M5G 1Y8
Canada
Phone: +1 (416) 925-5643
Fax: +1 (416) 925-0581
E-mail: sales@snowbush.com
Web Site: http://www.snowbush.com

MEXICO
288-A Paseo de Maravillas
Jesus Ma., Aguascalientes
Mexico 20900
Phone: +1 (416) 848-0328

JAPAN KK
Shinjuku Green Tower Building 27F
6-14-1, Nishi Shinjuku
Shinjuku-ku, Tokyo, 160-0023
Japan
Phone: +81 (03) 3349-5501
Fax: +81 (03) 3349-5505
E-mail: gennum-japan@gennum.com
Web Site: http://www.gennum.co.jp

TAIWAN
6F-4, No.51, Sec.2, Keelung Rd.
Sinyi District, Taipei City 11502
Taiwan R.O.C.
Phone: (886) 2-8732-8879
Fax: (886) 2-8732-8870
E-mail: gennum-taiwan@gennum.com

GERMANY
Hainbuchenstraße 2
80935 Muenchen (Munich), Germany
Phone: +49-89-35831696
Fax: +49-89-35804653
E-mail: gennum-germany@gennum.com

NORTH AMERICA WESTERN REGION
691 South Milpitas Blvd., Suite #200
Milpitas, CA 95035
United States
Phone: +1 (408) 934-1301
Fax: +1 (408) 934-1029
E-mail: naw_sales@gennum.com

NORTH AMERICA EASTERN REGION
4281 Harvester Road
Burlington, Ontario L7L 5M4
Canada
Phone: +1 (905) 632-2996
Fax: +1 (905) 632-2055
E-mail: nae_sales@gennum.com

KOREA
8F Jinnex Lakeview Bldg.
65-2, Bangidong, Songpagu
Seoul, Korea 138-828
Phone: +82-2-414-2991
Fax: +82-2-414-2998
E-mail: gennum-korea@gennum.com

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