



GS2989

Design Guide

Version	ECR	Date	Changes and / or Modifications
2	157313	December 2011	Corrections to the sink or source value for input and output pins in Section 4. Adjustments to Figure 2-1, Figure 2-3, Figure 2-4, Figure 2-5.
1	154995	September 2010	Removed "Proprietary & Confidential" from document footer.
0	151405	September 2009	New document.

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Overview

Together with the GS2989 Evaluation Board (EB-GS2989), the EB-GS2989 User Guide and the GS2989 Data Sheet, this document serves as a reference for designing with the GS2989, a Multi-Rate Dual Output Cable Driver. This document contains two main areas of focus:

1. Considerations in the schematic design.
2. Recommended PCB layout practices when designing with the GS2989.

Figure A below shows a typical GS2989 application block diagram.

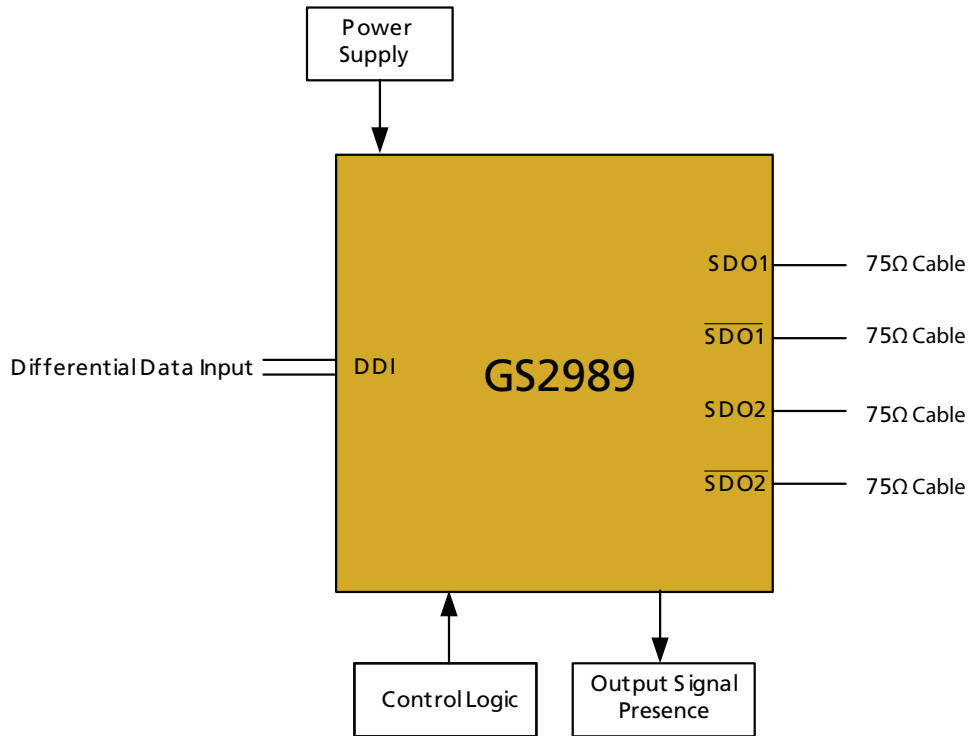


Figure A: Typical Application of the GS2989

1. Power

The GS2989 requires a single power supply at either 3.3V or 2.5V, provided a high output swing is not required. If a high output swing is required, the termination voltage should be capable of being connected to 5V, while the supply of the device remains at 3.3V or 2.5V.

The following guidelines are recommended when designing power for the GS2989:

- Use coupled power and ground planes i.e. use minimum spacing between power and ground planes. Power and ground planes form a natural capacitor, which will increase capacitance
- Do not overlap power planes. If it is unavoidable, different power planes should be isolated from each other with a ground plane between them
- Power and ground planes should be placed near the component side, which will reduce inductance of vias
- Bulk supply decoupling capacitors of 10 μ F and 100nF are recommended to filter-out high frequency noise
- It is recommended to decouple each power supply pin individually with a 10nF capacitor. All decoupling capacitors should be placed as close as possible to the power and ground pin pairs of the GS2989. Decoupling capacitors for the termination supply should be placed on the same side of the board as the GS2989 and as close as possible to the termination resistors. Wherever possible, use two vias for each VCC and GND pin and flood the copper area
- Central paddle should be connected to ground with multiple vias for proper thermal dissipation. At least 5 vias are recommended

2. SDI Input and Output

The GS2989 takes in 100 Ω differential input, and is capable of driving up to four 75 Ω single ended co-axial cables. The GS2989 can drive data rates up to 2.97Gb/s, and provides two selectable slew rates in order to achieve compliance to SMPTE 424M, SMPTE 292M and SMPTE 259M.

The following general guidelines are recommended when designing the transmission lines for the GS2989:

- Input and output trace lengths should be minimized and the input differential traces should be closely matched, and curved rather than sharp-angled
- Any discontinuity (ie. impedance transitions) should be avoided on the transmission lines
- No silk-screen should be allowed on these traces to ensure an accurate impedance
- 4.7 μ F ceramic AC-coupling capacitors are recommended for the input and output transmission lines as shown in the schematic

- Input transmission lines should have 100Ω differential controlled impedances, while output transmission lines should have 75Ω single-ended controlled impedances
- Non-transmission line components should be at a minimum distance of 10x the transmission line width (example: if transmission line is 1mm wide, the closest non transmission line component needs to be at least 10mm away)
- Antipads are recommended to deal with transmission line component parasitics. The antipad sizes used on the evaluation board are given in [Figure 2-1](#), [Figure 2-2](#), [Figure 2-3](#), [Figure 2-4](#) and [Figure 2-5](#). These antipad sizes are specific to this design, which uses ISOLA FR-410 dielectric with a 10mil thickness between the top routing layer and the associated GND and PWR plane layers. NOTE: Antipads are defined as the absence of copper in the underlying GND and PWR plane layers. As well, there should be no routing on any routing layer underneath the antipads

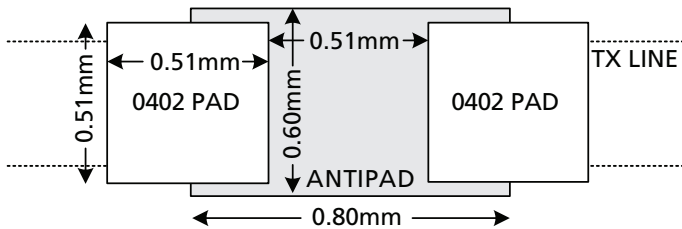


Figure 2-1: Series 0402 Component Antipad optimized for 50Ω traces

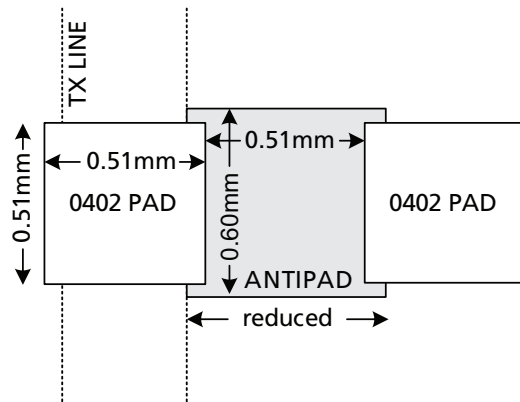


Figure 2-2: Shunt 0402 Component Antipad optimized for 50Ω and 75Ω traces

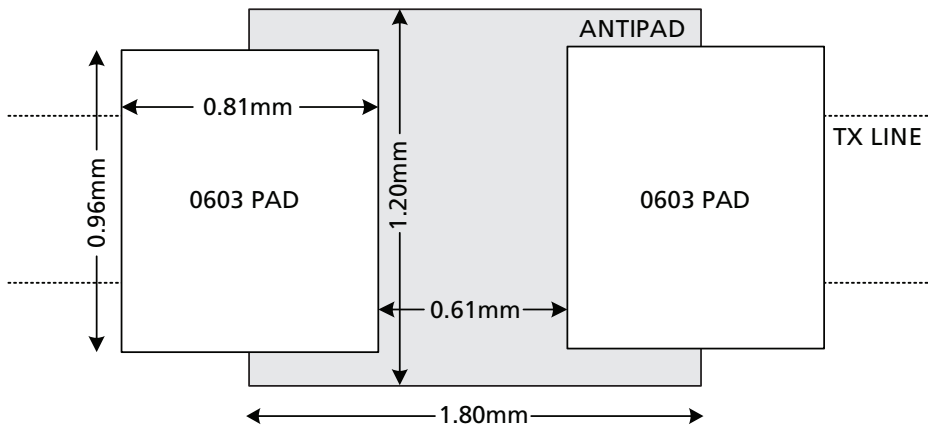


Figure 2-3: Series 0603 Component Antipad optimized for 50Ω traces

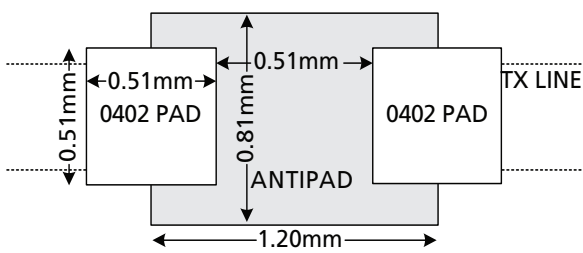


Figure 2-4: Series 0402 Component Antipad optimized for 75Ω traces

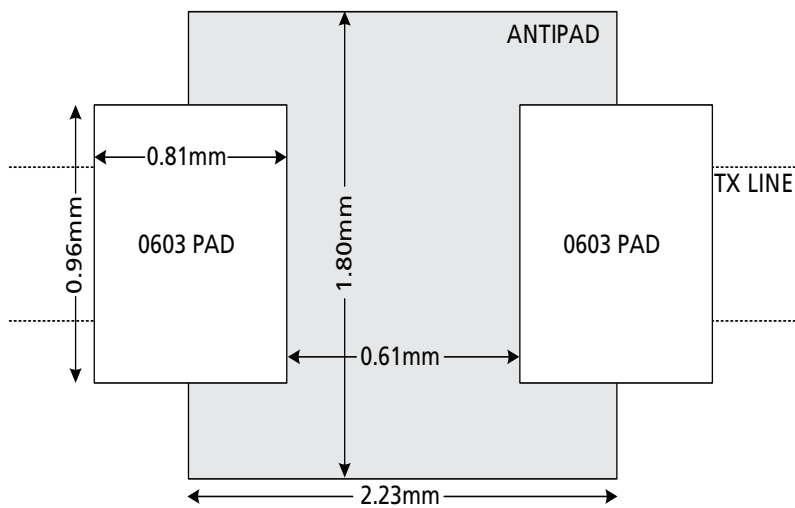


Figure 2-5: Series 0603 Component Antipad optimized for 75Ω traces

3. ORL Design Recommendations

This section contains recommendations that should be followed to obtain good Output Return Loss (ORL) when designing with the GS2989.

3.1 Termination Resistor Placement

It is recommended to place the termination resistors 4-5mm away from the device pins. The distance to the termination resistor will change the way the ORL compensation network is designed.

Generally, placing the termination resistor closer to the device improves the ORL and has the same effect as increasing the ORL network inductor value.

Placing the termination resistor farther away from the device improves the eye shape and has the same effect as decreasing the ORL network inductor value as shown in Figure 3-1.

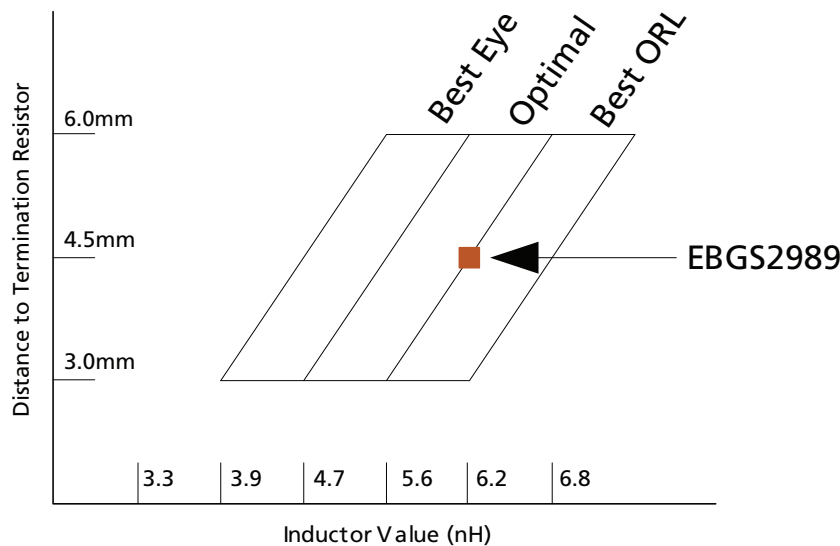


Figure 3-1: Termination Resistor Placement

To obtain a good trade-off between ORL and eye quality, the termination resistors should be placed no closer than 2mm away and no farther than 6mm away from the device. The evaluation board design uses a distance of 4.5mm.

3.2 ORL Compensation Network

The ORL compensation network should consist of a 75Ω resistor in parallel with an inductor. The optimum inductor value will depend on how far the termination resistor is placed from the device. See Figure 3-1.

The type of inductor used in the ORL compensation network is important for good performance. For best performance, select a chip inductor with good tolerance and high self resonant frequency, such as the LQG15HS series Murata inductors.

3.3 AC-coupling Capacitor

It is recommended to use a 4.7 μ F ceramic capacitor to AC-couple the outputs with a voltage rating of 10V or better. The pad size should closely match the transmission line width to avoid impedance discontinuities. It is also recommended to use antipads (absence of copper in the underlying ground and power planes) to compensate for the parasitic effects of the capacitor package.

3.4 Termination Voltage Decoupling

The termination voltage should be decoupled with 10nF ceramic capacitors. Decoupling capacitors should be placed on the same side and as close as possible to the termination resistors.

3.5 BNC Edge Connector Footprint

It is important to have a good BNC edge launch. The BNC footprint central pin should be as close as possible to the transmission line width and antipads should be used. Please refer to [Figure 3-2](#) for details on the footprint used in the evaluation board.

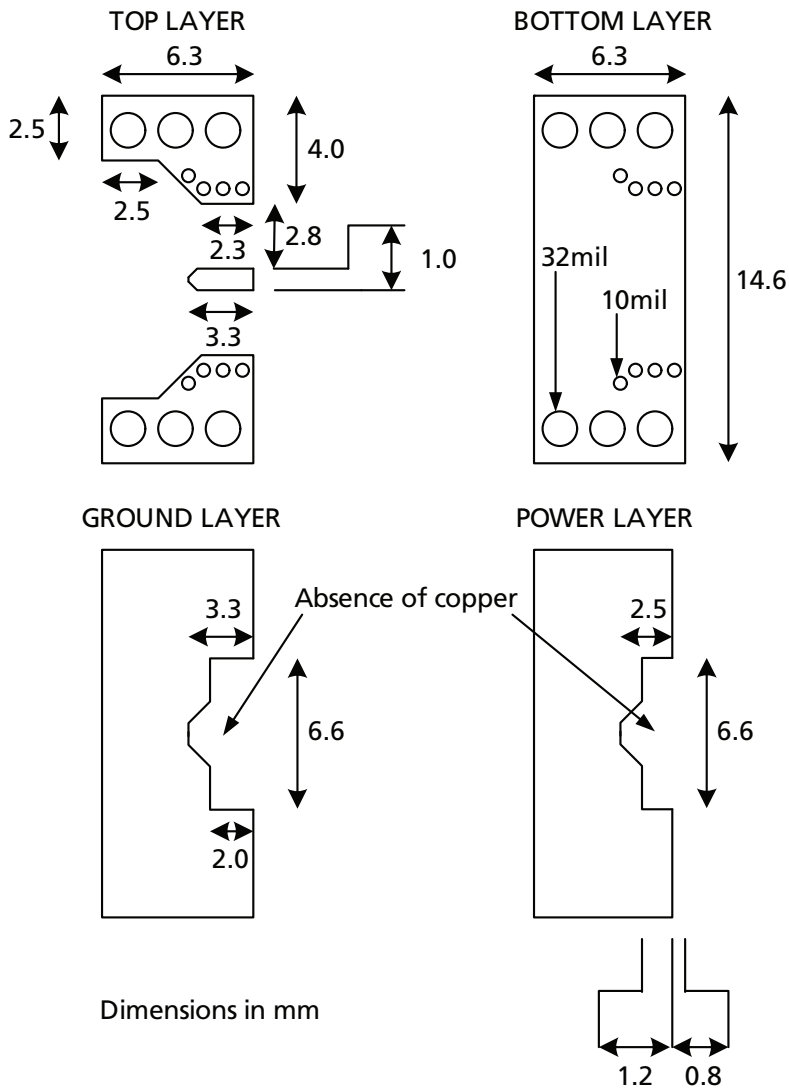


Figure 3-2: BNC Footprint

4. Other Considerations

- Input and output pins can only sink or source 2mA. Therefore, the $\overline{\text{OSP}}$ output pin should not be used to drive LEDs directly, LED drivers should be used instead.
- For good performance, the RSET resistor should be placed as close as possible to the RSET pin.

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DESIGN GUIDE**

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