Developments in Point of Load Regulation

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Point of load regulation has been used in electronic systems for many years especially when the load circuit is sensitive to noise. For example, in radio receivers it has long been a common practice to isolate sensitive loads from power supply noise by local linear regulation. When the first generation of powerful microprocessors appeared in desktop personal computers a Voltage Regulator Module (VRM) was required to regulate the low voltage high current supply to its core. It was impractical to use the centralised AC-DC converter or silver box due to resistive losses in cables, printed circuit board tracks and connectors. As the microprocessors became faster and more powerful the step change in current required to switch from one operating mode to the next presented another problem to the centralised approach, that of conductor inductance and the requirement for localised energy storage in the form of electrolytic capacitors. In the mid-80s Bell Northern Research coined the phrase "point of use power supply" (PUPS) for the modular DC-DC converters or bricks on line cards in telephone exchanges. This Distributed Power Architecture is shown in figure 1.
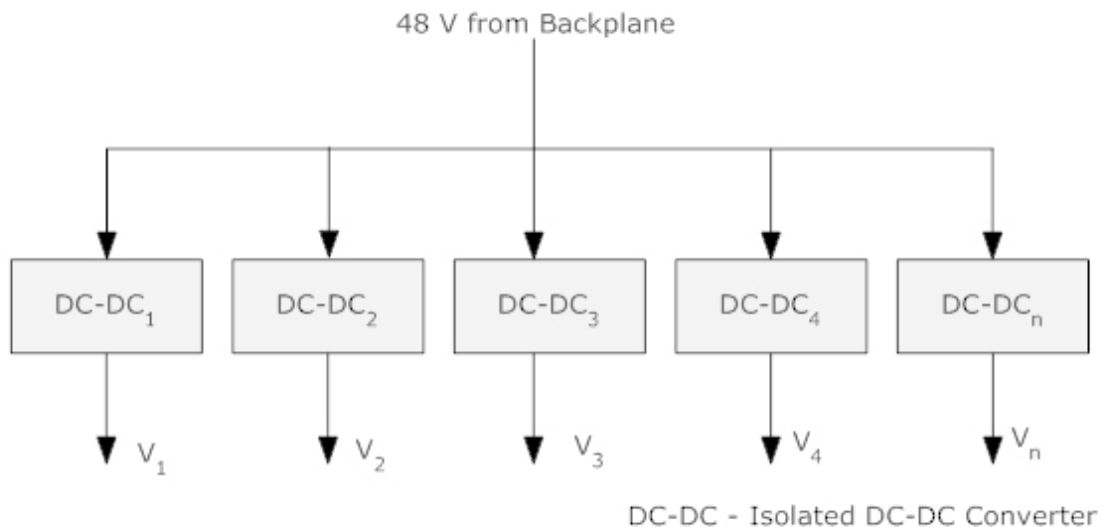

Figure 1 - Classic Distributed Power Architecture

Dedicated point of load regulators have been commonplace in military and aerospace applications where modularity and sub circuit isolation are required for reliability, serviceability and low susceptibility to

interference. So the concept of point of load regulation is not new, the reasons for its widespread adoption have become more compelling as the bandwidth content and functionality of electronic equipment has increased inexorably over time. The number of power supply rails on a system card has increased along with the complexity of the integrated circuits which make up the load. Furthermore, as we shall see later, the technology of the load integrated circuit load also has a strong influence on the electrical characteristics of the point of load regulator, particularly its ability to respond quickly to load transients.

CMOS integrated circuits are continually evolving utilising smaller line widths and feature size to pack more processing power and faster clock speeds into the same die area. Below 90 nm the quality of the transistors used in analog peripherals such as phase locked loops in transceiver circuitry is significantly degraded. Specifically the VI characteristic of the device becomes less useful from the analog perspective. These non-ideal characteristics manifest themselves as poor matching, common mode rejection and power supply ripple rejection. Furthermore circuit performance is also diminished by the IC designer's preference for single ended circuitry to conserve die area. There is also a strong economic incentive to push the problem into the power management solution; a deep sub-micron mask set costs over $1 million making system changes prohibitively expensive. The next generation of CMOS loads requires lightning fast transient response and settling time together with low noise and ripple. The point of load regulation solution should have wide control loop bandwidth and low dynamic output impedance so that any switching loads do not create ripple and noise at their power terminals.

As the number of power supply rails on the system card increased due to complex load circuitry system designers turned to the Intermediate Bus Architecture (IBA). This technique, shown in figure 2, was developed mainly for telecommunications and networking. At the edge of the card is an isolated bus converter which takes a distributed SELV voltage and creates a loosely regulated intermediate bus, which is delivered to a variety of point of load regulators. A mid range Ethernet router card can have as many as 30 independently regulated rails. Currently low power rails, typically below 1.5 A, are linearly regulated with low drop-out regulators (LDOs). However, recent limits imposed by the electrical utilities on overall system power together with consumer demand for increased bandwidth content and functionality have led designers to consider efficient switching regulators for all but the lowest power applications. If the input power to the system is limited or the ability to remove more than a certain amount of heat from the enclosure is constrained the only way to increase processing power is by more efficient power management solutions. As CMOS technology offers the power management IC designer increased current density and sophisticated control, steps are being taken to reduce the intermediate bus potential to below 6 V, the breakdown voltage of 5 V CMOS processes.
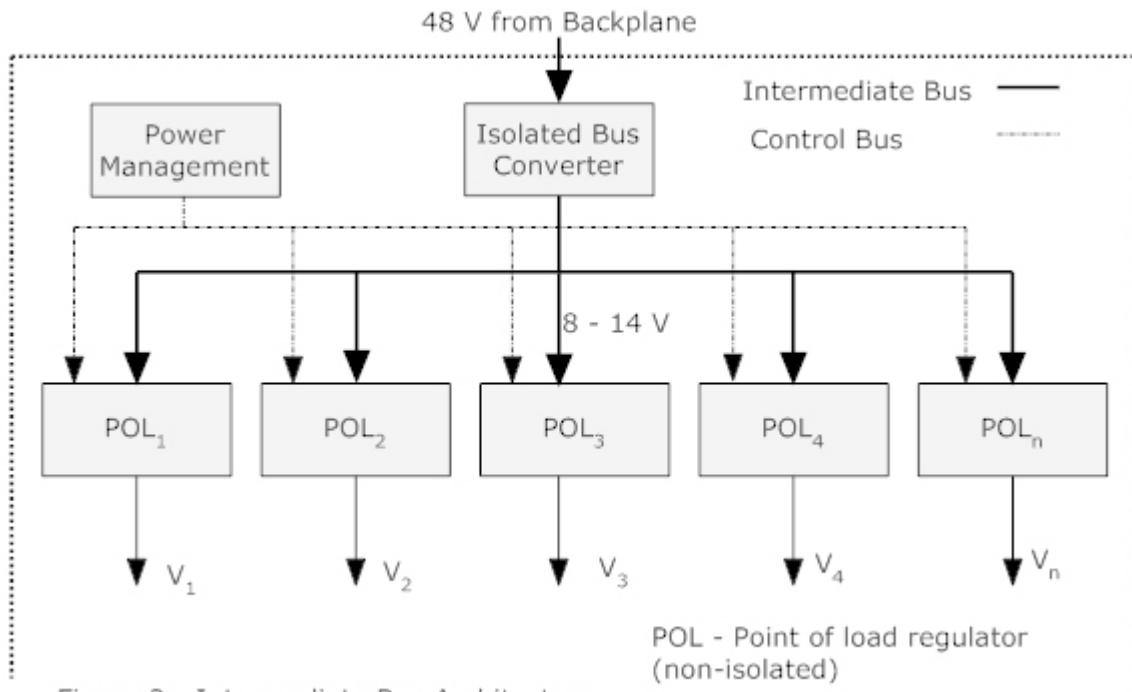
Figure 2 - Intermediate Bus Architecture

Currently there is a debate about centralised versus distributed control in distributed power architectures. In the Centralised Control Architecture, shown in figure 3, the point of load regulator has a digital interface and some programmability but no non-volatile memory. The control of the point of load regulator takes place through its digital interface from a central control IC, which is essentially a specialised microcontroller. The programming of the point of load regulator in the system sets up initial conditions and default settings in the event of an interruption of the control signal. Non-volatile memory at the point of load is considered unreliable in certain quarters as regulators dissipate heat.
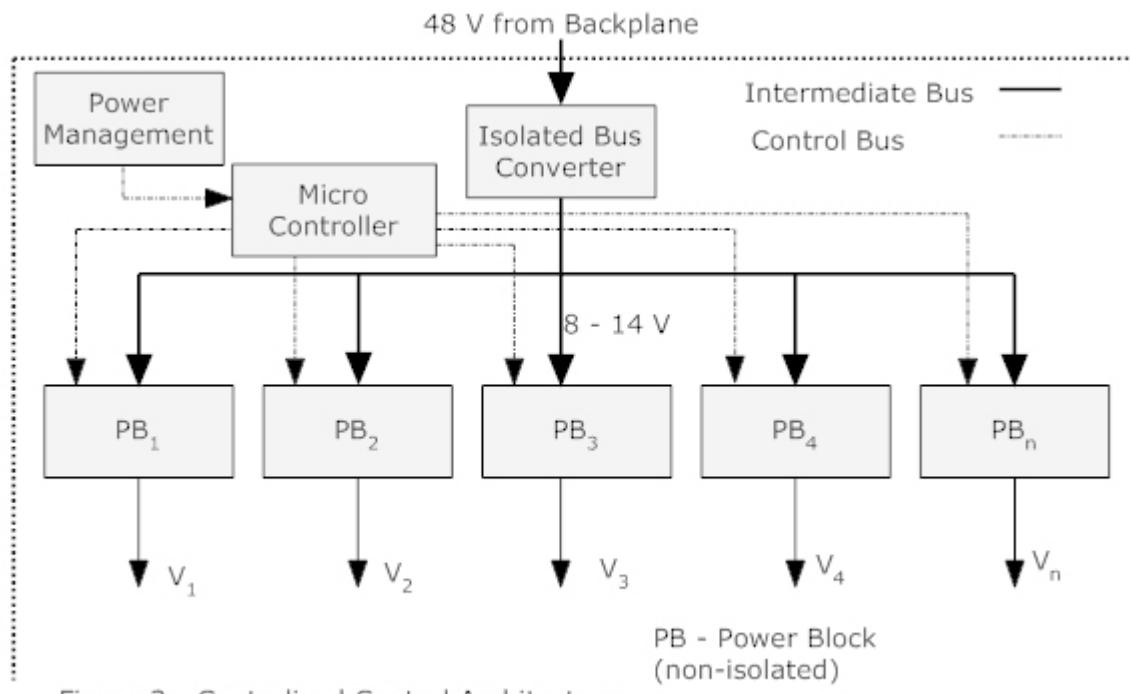
Figure 3 - Centralised Control Architecture

Another school of thought is that the point of load regulator is self-contained and runs its own control algorithm periodically reporting to a centralised watchdog or monitor IC. Each approach has its merits; however, customers generally want the centralised control architecture for mass production and the distributed control architecture for system development as this approach is the best value for money. Estimates from high-performance computing system engineers are that programmable power management solutions could potentially save six months of development and commissioning time speeding time to market. Another topic of interest to the system designer is that of failure prediction circuitry in the point of load regulator monitoring temperature at various points within the system and other variables such as ripple voltage amplitude could yield advance warning of a load circuit failure. Predictive failure analysis is of particular interest to high availability systems designers. In "five nines" reliable systems (with 99.999% availability) the ability to anticipate faults and conduct maintenance without expensive downtime is crucial. This technology is even available in today's office, many photocopier machines, which frequently provide network attached printing communicate independently to service companies. The first thing a user knows about the service is when the service engineer arrives to conduct a repair. This scenario is more important as companies begin to rely on remote storage and data processing on the web; the "cloud computing" environment.
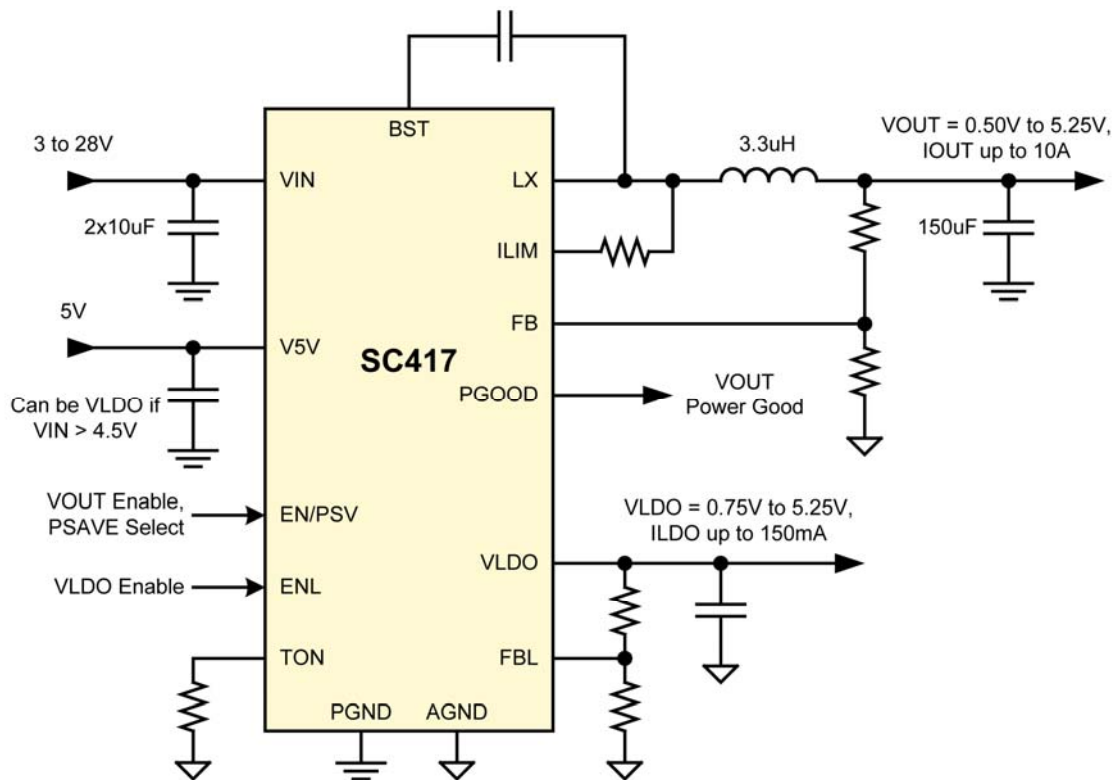
Figure 4 - SC417 point of load regulator application

The SC417 shown in figure 4 represents the culmination of many years of dedicated point of load regulator design. Hard-won expertise in powering dynamic high current, low voltage microprocessor cores in a variety of demanding applications has resulted in a low compromise solution, particularly when the power source is a semi-regulated power supply such as an ac adapter, the ubiquitous wall-wart. This solution provides the best control regulation and power switching technology in a 5mm x 5 mm QFN package. Constant ON-time control coupled with a driver which "tunes" itself to the MOSFET power switches minimising noise and overshoot provide a responsive solution which is compatible with the latest CMOS load technology. Point of load regulation is continually developing to match load technology and enable sophisticated applications. FPGA manufacturers wish to put the power supply in the package with its complex load. Delivering a product that runs from a standard power rail has its attractions; currently a major burden of FPGA applications support is troubleshooting power management issues. This level of miniaturisation is far from simple; the complete inductor assembly for such a product has to have a profile of less than half a millimetre to be feasible.

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