On-chip Jitter and system Power Integrity

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Abstract
On-chip Jitter induced by switching chip logic is often the reason why a device fails to achieve high operating frequency, or low bit error rate (BER). Therefore, research of on-chip Jitter is crucial for high speed design. In this paper, the method for measurement of on-chip Jitter is described. Using this method Jitter is studied in Frequency, Time, Spatial domains, and versus Decoupling. It is shown that the common approach to the reducing on-chip voltage variations and jitter by extensive decoupling on PCB leads to raising jitter instead of lowering it. It is demonstrated how Jitter peaks and PDN’ resonances might be evaluated through Jitter measurements. Using these data the system voltage variations are simulated in Time Domain for the stationary and non-stationary aggressor and victim; the Jitter behavior is evaluated base on simulations results. The paper describes practical methodology to measure on-chip jitter, evaluate PDN performance, and guide the design to achieve low noise and jitter in a system of Chip-Package-PCB-Decoupling.

Author Biography
Iliya Zamek is one of the pioneers in the field of Jitter. He started as an engineer and grew to system architect / project manager working on ATEs for VLSI, SRAM/DRAMs, and instrumentation in —Quartz, Russia’s leader in measurement and instrumentation equipment. He founded and led a startup, which evolved into a successful company. For over 15 years he worked for a leading Russian measurement Instrumentation Corporation “Quartz”, where he developed ATEs for VLSI, SRAM/DRAMs, and instrumentation, and progressed from engineer to system architect / project manager of comprehensive design projects. He founded a startup, which resulted in a successful company. In the US, he worked for a leading manufacturer of crystal oscillators, Q-Tech Corporation, where he designed many devices with Flight and Space rate requirements. He worked as a MTS in Altera Corp. and as a consultant for different companies, including Intel Corp. For the last 9 years, he has led R&D projects for nm-devices characterization and development, including research of on-chip Jitter and Signal and Power Integrity. He is currently a principal engineer with Semtech Corp., working on high speed Transceivers and Serdes devices. He received his BS and MS in Physics and Electronics, and a PhD from Nizhniy Novgorod State University. He has published more than 50 papers, and has been granted 20 patents.
1. **Introduction. Undesired effects limiting performance of modern nm-devices**

The success of nm-technology for the last decade has made available high speed nm-devices. However, potentially achievable high nm-devices’ speed turned to be limited by new undesired effects revealed in nm-ICs: noise and timing variations of internal chip signals, or jitter, due to switching on-die logic [1-6]. Internal chip logic of any IC has various logic domains switching at different moments of time. Some of these logic regions might be considered as aggressors for other chip logic domains, which become victims if they share the same power supply or return pass with an aggressor. At aggressor switching from one logic state to other, it consumes a pulse of a current. The current pulse causes voltage variations $\Delta V_{PDN}(t)$ on power rails inside the chip. These voltage variations, next in turn, cause timing variations of internal chip signals of a victim. As a result, internal chip signals experience the additional deterministic Jitter which we name “parametric”, or “power induced” jitter $DJ_p$. For this reason, the implementation of high speed nm-devices and, in particular, their decoupling, requires research noise and jitter inside the chip.

The older generation of ICs with elements size 180 nm and higher did not have significant current variations inside and from this point might be considered as quiet, without internal voltage variations on power rails. It was possible not to account for the PDN noise inside these chips. Therefore, the decoupling methodology for these devices was just to guard them from the external noise sources, Figure 1a. With chip elements scaling down, new sources of noise appeared, and these noise sources occur inside the chip, – Figure 1b. This new situation required a new approach to devices decoupling.

Another important problem to study is how PDN voltage variations affect the chip internal signals’ timing. The impact of power voltage variations on chip signals waveform and timing has a parametric and non-linear character. Both problems: analysis of system Power Integrity, and research of how PDN voltage impacting chip timing, are complex.

The goal of this paper is to avoid noted troubles at research of chip noise and timing and develop a practical approach to the system PDN and $DJ_p$ evaluation, modeling and reduction. This approach includes particular, the evaluation of PDN noise and Jitter properties at periodic type of aggressor first, and then, implementation obtained results to study of noise and Jitter for more complex cases of the non-stationary aggressor.

In section 2 of the paper the on-chip Jitter generation mechanism is studied. The effect of a doubling aggressor frequency impacting the victim is introduced. In section 3 the Aggressor and Victim frequencies

![Figure 1. On-chip noise: a) - external noise for the quiet chip; b) – internal noise sources due to toggling on-chip logic appeared inside high speed devices.](image-url)
relationships that provide the max and min Aggressor impact to the Victim are explained. The method for on-chip Jitter measurements at periodic aggressor and victim is described. Using this method, the paper further presents: a jitter resonance revealed in a system of Chip-Package-PCB-Decoupling capacitors [7]; Spatial Jitter behavior over the chip die – section 4; on-chip Jitter behavior versus decoupling – section 5. Theoretically and experimentally, research demonstrates that the common approach to the reducing PDN noise by extensive on-board decoupling leads to rising jitter instead of lowering it. In section 6 the described method is implemented for the evaluation of PDN resonance frequencies through Jitter measurements. Using obtained data about PDN resonance frequencies, the PDN noise inside the die simulated with Time Domain approach for the non-periodic aggressor cases. The examples of the simulation are described in section 7, where the on-chip victim noise and jitter behavior studied. In section 8 the possibilities of the reducing on-chip Jitter in advanced technologies is discussed.

Overall, the results of this paper represent a practical approach to study on-chip Jitter, evaluate PDN performance, and predict noise and Jitter that allow to achieve reduced design’ noise and jitter through improving the Power Integrity and prediction of the on-chip Jitter behavior.

2. Frequency and Time Domain approaches to the analysis processes in a PDN

2.1. Frequency and Time Domain approaches to the PDN analysis

Different aspects of a PDN were studied in numerous publications. The main focus of these works was PDN complex impedance \( Z_{PDN}(f) \) that defines, together with chip current waveform, the voltage variations on chip power rails. For calculations of the voltage variations inside PDN next equations are commonly used in Frequency Domain [8-11]:

\[
\Delta V_{PDN}(f) = Z_{PDN}(f) \times \Delta I(f)
\]

(1A),

and in Time Domain (see [11-13] and references):

\[
\Delta V_{PDN}(t) = \int_{0}^{t} Z_{PDN}(t - \tau) \times \Delta I(\tau) \cdot d\tau
\]

(1B)

Functions \( \Delta V_{PDN}(f), Z_{PDN}(f), \) and \( \Delta I(f) \) are Fourier transforms of: \( \Delta V_{PDN}(t) \) - voltage variations inside the chip in time domain; \( Z_{PDN}(t) \) - PDN transfer impedance; \( \Delta I(t) \) - chip current variations in time domain.

Direct implementation of these equations meets some difficulties associated with complexity of the system and lack of information about system parameters. Therefore, there appeared some limitations in these approaches:

- using Frequency Domain (FD) approach at PDN analysis most researches ignore the phase frequency dependence \( \phi_z(f) \) of PDN complex impedance \( Z_{PDN}(f) = Z(f) \cdot \exp(i \cdot \phi_z(f)) \). Also, at research Jitter induced by power noise, some authors use FD approach with sine wave type of an aggressor for the noise analysis first; then, the impact of a different aggressor’ frequency harmonics are combined to study the noise and Jitter. This two step process complicates the research;
- at Time Domain (TD) approach to the PDN analysis the order of the differential equations that describe the real system behavior became very big. These mathematical troubles forced researchers to use simplified models, which bring some inaccuracies when using TD methodology;
- in publications that analyzed PDN with both FD and TD approaches have not paid enough attention to the specific of the PDN as a linear time-varying (LTV) system.

In this work practical methods are introduced that help to avoid noted troubles at both these approaches by implementation of PDN noise simulations, supported by measurements of the system PDN resonance frequencies.
2.2. Dynamic current in CMOS devices and effect of a doubling aggressor frequency impacting the victim.

In a digital chip only two types of signals exist inside: transition from logic 1 to 0 and from 0 to 1. Therefore, it is natural to build the research of processes in a PDN base on these elementary signals only, rather then on sinusoidal signals. During the transition, each internal chip element produces pulses of a current corresponding to the rising and falling transitions of a signal. At chip operation its numerous logic elements (LE) are switching at different moments in time, as upper graph on Figure 2a illustrates; current pulses that belong to one logic element marked by the same color. The research of the Dynamic current inside a chip [10] shows that current pulses due to the aggressor’ rising and falling edges have slightly different amplitude and width, Figure 2b. This difference might happen due to various rise and fall time of the switching logic elements, and/or difference in clocks’ delays that are used for each logic element synchronization, etc.

The impact of the aggressor current pulses on PDN noise was not fully studied in [10]. Let consider Dynamic current of a chip in more details. Name current pulses that correspond to the rising and falling aggressor edges as “odd” $I_{odd}^{i}(t - t_{2n+1})$ and “even” $I_{even}^{i}(t - t_{2n})$. The total current flow of a chip might be presented as a sum of two parts – one with all Odd and other with all Even pulses, see lower pictures on Figure 2a. For the current of one LE we can write:

$$\Delta I(t) = \sum_{n=0}^{N} I_{odd}^{i}(t - t_{2n+1}) + \sum_{n=0}^{N} I_{even}^{i}(t - t_{2n+1})$$  \hspace{1cm} (2)$$

Where $N$ - is a number of current pulses observed, and $t_{n}$ - are the aggressor switching moments.

In [10] numerous flip-flops (TFFs) in Core logic switching simultaneously were used as an aggressor. In this case, all current pulses that belong to different LEs will be grouped in time and total aggressor current pulses’ amplitudes rises, as it is shown on Figure 2b. As we see, there are two aggressor’ current pulses happening during each period of switching aggressor logic – Odd and Even. As a result, the frequency of an aggressor

![Figure 2. On-chip Dynamic current: a) illustration of the Even and Odd current pulses due to toggling Core logic elements inside the chip; b) simulated Dynamic current waveform inside the chip of simultaneously switching flip-flops [10].](image-url)
impact to the PDN is doubling. Assume that aggressor logic is switching periodically with period $T_{SW} = 1/F_{SW}$. For simplicity, we suppose that there is no difference in Even and Odd current pulses amplitudes. So, as there are two current pulses corresponding to each aggressor switching logic period $T_{SW}$, the current pulses period $T_A$ is two times less compared to the aggressor switching logic’ period: $T_A = T_{SW} / 2$. Consequently, an aggressor frequency $F_A = 1/T_A$ is two times higher compared to the frequency of switching aggressor logic: $F_A = 2 \cdot F_{SW}$.

We will be using the definition of the aggressor frequency as a frequency of switching current pulses $F_A$.

2.3. Analysis PDN voltage variations at Periodic Stationary Aggressor

PDN voltage variations can be calculated with substitution (2) in equations (1). Without making distinctions between current amplitudes, we can write for the voltage variations in a PDN:

$$\Delta V_{PDN} (t) = \sum_{n=0}^{N} \int_{0}^{t} Z_{PDN} (t - \tau) \cdot I(\tau) \cdot d\tau$$  \hspace{1cm} (3)

Where $N$ is a number of pulses observed. We can rewrite (3) next:

$$\Delta V_{PDN} (t) = \sum_{n=0}^{N} H_{PDN} (t - n \cdot T_A)$$  \hspace{1cm} (4)

Where $H_{PDN} (t) = \int_{0}^{t} Z_{PDN} (t - \tau) \cdot I(\tau) \cdot d\tau$ - is a convolution of current pulse waveform and PDN’ transfer impedance.

As it follows from (3) and (4), PDN voltage variations represent the equivalent “filtering” of an impedance transfer function $Z_{PDN} (t)$ with pulse waveform $I(t)$.

3. On-chip Victim Jitter at periodically switching Aggressor

3.1 Min/Max Victim Jitter versus Aggressor and Victim frequencies relationships

It was shown [14, 15] that aggressor impact to the victim depends on aggressor and victim frequencies relationships. There is an unlimited number of frequencies of aggressor $F_A$ and victim $F_V$ combinations to investigate. However, when aggressor and victim are switching periodically (even at more general asynchronous aggressor and victim cases), it is possible to find frequencies relationships, which provide maximum and minimum aggressor impact on victim timing. This can significantly reduce the volume of the required measurements. Let us consider an aggressor impact on rising victim edges.

Asynchronously switching aggressor and victim.
Victim Jitter versus asynchronously switching Aggressor and Victim studied in [14-16]. It was revealed that Victim timing behavior is different when $F_A \geq F_V / 2$, and when $F_A < F_V / 2$.

In a first case, when $F_A \geq F_V / 2$, there exist next frequencies combinations with maximum and minimum aggressor impact on victim:

$$F_A^{MAX} = F_V \cdot (k + \frac{1}{2}) \quad k = 0,1,2,3,...$$  \hspace{1cm} (5A)

$$F_A^{MIN} = F_V \cdot k \quad k = 1,2,3,...$$  \hspace{1cm} (5B)
Where $F_{A}^{MAX}$ - are Aggressor frequencies at which Aggressor provides maximum impact on Victim’ Jitter, and $F_{A}^{MIN}$ - are Aggressor frequencies with minimum Aggressor impact on Victim’ Jitter.

At $F_{A} < F_{v} / 2$ there are also will be observed frequencies relationships with maximum victim Jitter and minimum Jitter at frequencies between these maximums:

$$F_{A}^{MAX} = \frac{F_{v}}{k}$$

$k = 3, 4, \ldots$ (6)

Figure 3 illustrates some of the important cases of the aggressor and victim frequencies $F_{A}$ and $F_{v}$ relationship. Remember, that we are considering the asynchronous case when aggressor and victim are moving in respect to each other; the Figure shows the instantaneous aggressor and victim positions. On Figure 3a, at $F_{A} = F_{v}$, an aggressor impacting similar all victim’ rising edges, therefore, in this case victim experiences minimum timing variations of one rising edge respect to other rising edge. Otherwise, in the case presented on Figure 3b, when $F_{A} = F_{v} / 2$, victim’ timing will be strongly affected: each clock’ odd rising edge will experience an aggressor impact, but each next rising edge will be affected less due to lack of corresponding aggressor current pulse. Therefore, neighboring victim rising edges will be impacted by aggressor differently which makes this case the worse from the point of victim timing variations. The last one confirmed by Figure 3c where each fours victim rising edge will be affected by aggressor, while each second and third rising edges affected less; this case when $F_{A} = F_{v} / 3$ also exhibits maximum victim jitter, but its value is less compared to case on Figure 3b due to less number of victim edges affected by aggressor current pulses. The private case at $k = 0$ in (5A) provides the worse case impact of periodic aggressor on the periodic victim’ timing. We name this case “F/2 rule” and used it for the victim Jitter measurement method that we describe in the next sections.

Consider synchronous case versus asynchronous switching aggressor and victim. Being asynchronously, the aggressor and victim will be “moving” along each other, as we noted above. This movement might be slow at stable aggressor and victim frequencies. However, it brings some additional specific to the victim timing. For example, consider case presented in Figure 3a, when victim has minimum timing fluctuations. This relative movement of an aggressor still will not cause victim timing variations one edge respect to other. However, when aggressor pulses “match” the rising aggressor edges all victim pulses will be shifted in a clock Tree, and when aggressor pulses will not “match” the victim rising edges positions, all victim pulses will return

![Figure 3. Illustration of the aggressor and victim frequencies relationships: a) $F_{A} = F_{v}$ – there is minimum victim timing variations; b) $F_{A} = F_{v} / 2$ – maximum victim timing variations; c) $F_{A} = F_{v} / 3$ – significant victim timing variations are possible.](image-url)
to their original positions. So, the internal Clock Tree’s signals will not be distorted, but might change all clocks positions simultaneously and cause the shift of all synchronization signals inside the chip. In such cases a double image of a chip output signal is observed on an oscilloscope.

For the case of synchronous aggressor and victim, this effect will cause some phase dependence of on-chip Jitter versus relative aggressor and victim positions.

### 3.2 Measurement method of worse case victim jitter. F/2 Rule

Using equations (5) one can significantly reduce the measurement volume for the on-chip Jitter evaluation: instead of the measurement jitter at all possible aggressor and victim frequencies combinations, it is possible to evaluate it at worse case among all other cases, which happen at \( k = 0 \) in (5A): \( F_A^{\text{MAX}} = F_V / 2 \). Using this rule, a measurement method for on-chip jitter measurements was designed [14, 16]. This method has been widely used at various Signal Integrity issues in [14], at analysis worse case Jitter induced by simultaneously switching outputs of I/O [16], and to study Jitter due to Power noise at switching Core logic [17, 18].

The method is described in [18], where it was implemented for detail Clock Tree jitter evaluation inside a 90-nm FPGA. In the FPGA, one of the clock signals was chosen as a victim, and the switching logic pattern in core logic was used as aggressor. The Victim Clock (marked red on Figure 4a) is routed from the die left to the centre before leaving from the top right of the FPGA device. Separate pulse generators implemented as stimulus signals for the aggressor and victim, and there was no synchronization at all between the aggressor and victim. The same FPGA logic pattern with TFFs was used as an aggressor, as in [10] (see section 2.2 of this paper). The resulting victim timing variation was measured at the victim output with a real time oscilloscope, and is termed Core Jitter (parametric jitter \( DJ_P \) the more correct name). An aggressor created current pulses toggled at half the Victim Clock’s frequency according “F/2 rule”.

Figure 4b shows the measurement results for the Sigma victim’ Period and Cycle-Cycle jitter. Jitters measurements are normalized with respect to quiet jitter (Jq) when aggressor was not switching. When Victim frequency \( F_V \) changed, the Aggressor frequency \( F_A \) also followed, remaining equal to the half of the Victim frequency. Therefore, each point on the graph on Figure 4b represents the worse case jitter for each combination of victim and aggressor frequencies, according to (5A). In spite of relatively small logic utilization, we see a significant increase of jitter at switching aggressor versus case when aggressor was quiet – dashed lines.

![Figure 4](image_url)
We also see from Figure 4b that among all these worse cases, there are some outstanding at frequency of approximately 36 MHz due to PDN system resonance.

4. Jitter properties in a Spatial domain

It is important to know if Jitter measured by this method characterizes timing uncertainties of signals averaged over the chip, or they are carrying information directly from the affected small regions inside the die. To answer these questions, the following experiments were done [18]: the aggressor was localized in each one of a 9 zones inside 3x3 quadrants on which whole area of a die was “divided”; victim Jitter measured at all 9 aggressor’ locations sequentially; at each experiment aggressor localized in one of these 9 zones. The victim layout inside the chip was the same for all 9 experiments. Measurement results for victim Peak-to-Peak Period jitter from different Core Noise locations presented on Figure 5. We see that Jitter vary depending on different aggressor and victim relative locations. Maximum Aggressor impact to the victim timing happen when aggressor and victim share the same chip area: when victim input the chip - “left” aggressor and victim location; this curve marked purple. Next strongest impact happen when aggressor takes “Top right” position and share chip area where victim exit the chip; this curve marked red. From these experiments, it follows that described measurement method carries information about voltage variations from local area deep inside the chip die.

![Graph](image)

Figure 5. Results of the on-chip parametric jitter $DJ_p$ measurements versus relative aggressor and victim positions: a) Peak-to-Peak victim Period Jitter; b) Sigma Period victim jitter.

5. System Jitter properties versus PCB decoupling

5.1. Measurement experiments with decoupling

Lowering the PCB PDN impedance by increasing the decoupling has been a general recommendation for years to improve the system performance. However, we will show that this approach does not work in a resonance case. For the experiment we used same PCB with FPGA, as described in section 4, with 50 decoupling capacitances for the PCB Core logic power supply organized in three groups that were placed differently on the PCB respect to the IC [7] (see Table lower):

40 capacitances 0.1 µF, package 0402; 5 capacitances 1 µF, package 0603; 5 capacitances 10 µF, package 0805

First, we measured jitter with all decoupling capacitances included. Then we removed some capacitances and measured jitter again, Figure 6. We continued the experiments until some variations of a resonance curve were noted. The capacitances used in each experiment are shown in Table. As we can see from Table and Figure 6,
removing decoupling capacitors doesn’t cause the resonance frequency to shift even when the total capacitance of the decoupling system is decreased from 59 µF to 4 µF—more than 14 times. Decreasing decoupling further causes a small resonance frequency shift to the lower frequency. The frequency shift of the resonance became more significant when number of the decoupling capacitances and total capacitance became very small. It is interesting to compare experiments #1 with #4 and #5 in the Table. In the experiment #4 the total capacitance was reduced significantly, but number of 0402 capacitances and their vias were the same as in experiment #1; the resonance frequency was shifted just 1 MHz down with removing five 0805 and five 0603 type capacitances. In case #5 the total capacitance value was changed insignificantly, but the number of capacitances 0402 type and associated vias were reduced twice compared to experiment #1; this resulted on higher resonance shift—on 2 MHz down. The reason is that capacitances 0402 were placed closer to the package and the equivalent series inductance (ESL) of their connections to the chip was lower, compared to other capacitances; this makes the PDN resonance more sensitive to number of the closest capacitances.

<table>
<thead>
<tr>
<th>Number decoupling capacitances used in experiments</th>
<th>$f_{res}$</th>
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<tr>
<td>#</td>
<td>10 µF 0805</td>
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<tr>
<td>1</td>
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Figure 6. Measured victim Period Jitter due to switching aggressor core logic versus number of decoupling capacitors of the core VCC power supply: a) Period victim Jitter experience a resonance; b) detail shape of the resonance peak.
We also see from Figure 6 that jitter at low frequencies and, especially, at frequencies above 100MHz increases with lowering decoupling. This contradicts with common conclusion that decoupling capacitances are not working at frequencies above 100-200MHz. The last one illustrates the fact that capacitances at high frequencies are working as an inductances: at big number of capacitances their equivalent series inductances, which are included in parallel, reduce the PDN impedance.

Similar to the resonance frequency, the value of the resonance peak does not change significantly until the number of the decoupling capacitors was reduced 10 times. The peak value decreased in the last case, see Figure 6a, only when total capacitance reached 0.5 µF, which is impractical.

The most important conclusion from these experiments is that the traditional approach to reducing PDN noise by increasing the decoupling does not help to remove jitter resonance peak. Moreover, lowering the PCB impedance by adding more capacitances makes the situation even worse; the value of the peak increases.

5.2. System’ resonance frequency dependence versus number of the decoupling capacitances

The results of experiments with capacitances described in the previous section are supported by the following theory. Consider the case when we have many decoupling capacitances, say \( m \), placed at the same distance around the chip, Figure 7a. On the real PCB, a combination of different decoupling capacitors is used usually. However we are intentionally limiting our consideration by this simple case to help us clearly illustrate the main system properties. We may present the equivalent circuit of the PDN of a system with \( m \) capacitances as a simple lumped element model showed on Figure 7b. On this figure, the \( L_1 \) and \( R_1 \) are the system equivalent series inductance (ESL) and equivalent series resistance (ESR) associated with die, package, package ball, package mounting effect, vias to power and ground planes, etc. The \( C_d \) is total capacitance of all decoupling capacitors, and \( R_d \) and \( L_d \) are the total ESR and ESL of the decoupling capacitors, including resistances and inductances of a capacitors mounting pads, spreading inductances and resistances on power and ground PCB planes, and vias to power and ground planes. All these parameters define the system resonance. Assume that all decoupling capacitances have the same parameters ESL, ESR, C and equal traces and vias on PCB.

As decoupling capacitances are connected in parallel, its total capacitance increases \( m \) times; otherwise, total ESR and ESL (including mounting inductance, and spreading inductance on the PCB)
reduces \( m \) times:

\[
L_d = \frac{L_0}{m}; \quad C_d = C_0 \cdot m; \quad R_d = \frac{R_0}{m}
\]  

(7)

Where \( L_0, R_0, \) and \( C_0 \) parameters associated to one decoupling capacitor. Using (7), we can write for the system resonance frequency neglecting small \( R_{\text{die}} \):

\[
 f_{\text{res}}^{\text{Sys}} \approx \frac{1}{2\pi \sqrt{L_1 \cdot C_{\text{die}} \cdot \left(1 + \frac{L_0}{L_1} \cdot \frac{1}{m}\right) \cdot \frac{1}{1 + \frac{C_{\text{die}}}{C_0} \cdot \frac{1}{m}}}}
\]

(8)

Assuming that \( C_d >> C_{\text{die}} \), and number \( m \) of the decoupling capacitances is big enough, we can simplify last equation for the system resonance frequency:

\[
 f_{\text{res}}^{\text{Sys}} \approx \frac{1}{2\pi \sqrt{L_1 \cdot C_{\text{die}}}} \left(1 - \frac{L_0}{L_1} \cdot \frac{1}{2m}\right)
\]

(9)

From (9) it follows, that at big number \( m \) decoupling capacitances, the second member in the brackets becomes small and increasing decoupling by raising number \( m \) of the decoupling capacitances does not affect the system resonance frequency much. This is exactly what we observed in our experiments.

6. PDN resonances evaluation through Jitter measurements

The method described above is very effective for on-chip jitter evaluation. From another point, this method might be used for the evaluation PDN and its resonances. To research PDN properties through jitter measurements, the Period and Cycle-to-Cycle are preferable jitter terms, while we also might measure any jitter terms, like time interval error (TIE), etc. Let us consider why using of victim’ Period, or Cycle-Cycle jitter which is a first difference of period variations [14], are preferable at PDN study. As it is shown in [15], Jitter at the output of a linear system depends on the measured jitter term, system jitter transfer function \( |H(f)|^2 \), and input signal jitter spectrum \( S_n(f, F_A) \) which in our case will depend on aggressor frequency \( F_A \). Using the input jitter spectrum and system jitter transfer functions, we may write sigma jitter at the system output:

\[
\sigma_{\text{term}} = \left[ \int_{f_l}^{f_h} |H(f)|^2 \cdot S_{n_i}(f, F_A) \cdot P_{\text{term}}(f, F_y) \, df \right]^{0.5}
\]

(10)

where \( f_h \) is a cutoff frequency of the measurement instrument or in jitter spectrum; \( f_l \) is the lowest frequency at jitter measurements; and the so-called parameter function \( P_{\text{term}}(f, F_y) \) depends on measuring a particular jitter term which depends on victim frequency \( F_y \). The relations between jitter spectrum and different jitter terms like Period, Cycle-to-Cycle, and TIE have been studied in [14, 15]. As it was shown, jitter spectrum is multiplied by next parameter functions for different jitter terms:

TIE:

\[
P_{\text{TIE}}(f) \equiv 1
\]

(11A)

Period jitter:

\[
P_p(f) = 4 \cdot \sin^2 \left( \pi \frac{f}{F_y} \right)
\]

(11B)
Cycle-to-Cycle jitter: 

\[ P_{c-c}(f) = 16 \cdot \sin^4(\frac{\pi f}{F_v}) \] 

As we saw in section 2.2, the aggressor current pulses on Figure 2b will cause in jitter spectrum \( S_V(f, F_A) \) two components: strong harmonics at aggressor switching frequencies \( k \cdot F_A, (k=1, 2, 3 \ldots) \) marked orange on Figure 8a, and smaller harmonics with frequencies \( n \cdot F_{sw}, (n = 1, 2, 3, \ldots) \) marked by blue which appear due to the difference in odd and even current pulses amplitudes. The parameter function of Period and Cycle-Cycle jitter terms works as a filter with periodic characteristic in frequency domain that helps to separate and underline the even harmonics \( (2k+1) \cdot F_A, (k=1, 2, 3 \ldots) \) in victim jitter spectrum (marked orange on Figure 8b) and reduces further relative contribution of the harmonics with frequencies \( n \cdot F_{sw} \) (marked by blue). This is exactly what we need – to separate harmonics in Jitter spectrum with frequencies \( (2k+1) \cdot F_A \). So, the described measurement method helps to separate even harmonics in Jitter spectrum and measures the worse case Jitter among all possible aggressor and victim frequencies combinations.

\[ S_V(f, F_A) \]

\[ S_V(f, F_A) \cdot P_{term}(f, F_v) \]

**Figure 8.** a) Victim jitter spectrum due toggling aggressor; b) Equivalent victim jitter filtering at Period jitter measurements at \( F_A = F_v / 2 \).

When we are changing victim frequency at the measurements, the aggressor always follows to provide the worse case aggressor impact. When aggressor frequency matches the system resonance, its’ current pulses amplitudes rise, and Jitter experience a resonance peak, like on Figures 4b and 6. Registering this Jitter peak’ frequency is a simple way to evaluate the resonance frequency of a PDN respect to the chip die.

7. **On-chip PDN noise and victim jitter at non-periodically switching Aggressor**

7.1 On-chip PDN noise

There are many situations when aggressor inside the chip switching non-periodically: data signals in data buses are non-periodic; at interrupting clock activities; starting and stopping of reading and writing cycles of the memory; at power gating, etc. As we noted above, the direct analysis of a non-stationary case is complex. To escape these complexities we used the next three steps to approach this problem [18]: first, we evaluated system Jitter as it is described in sections 3.2 and 6; second, the system PDN resonance frequencies were defined base on Jitter measurement results; third, the PDN voltage variations on the chip’ die were modeled using Time
Domain approach. The PDN voltage waveforms at complex aggressor pattern are presented in [17]. Now we consider some simple examples to illustrate typical on-chip noise and Jitter behavior at non-stationary aggressor. Solving differential equations of a circuit on Figure 7b we can write the system transient response to one aggressor transition:

$$
\Delta V(t) = \Delta V_i \cdot e^{-\alpha t} \cdot \cos(\omega_0 \cdot t + \theta)
$$

(12)

Where $\Delta V_i$ is initial PDN voltage drop on chip' die power rails; $\alpha$ - is a decay factor, $\omega_0$ and $\theta$ are frequency of the oscillations and an initial phase. The voltage drop $\Delta V_i$ on the chip’ die due to aggressor transition depends on the aggressor current (width, amplitude, and shape), transitions’ pre-history, PDN parameters, and oscillations frequency $\omega_0 \approx 2\pi \cdot f_{res}$. The PDN’ transient response for the case of the relatively low decay time $1/\alpha$ compared to the oscillation period $T_{res} = 1/f_{res}$ is presented on Figure 9a. At aggressor transition the PDN voltage drops. Then, the PDN voltage starts rising, reaches the first maximum, oscillates and decays. Consider three cases when time between two consecutive aggressor transitions $T_i$ :

1. $T_i$ significantly exceeds decay time $T_i >> 1/\alpha$ and period oscillations $T_i >> T_{res}$, Figure 9a;
2. $T_i$ is significantly less then period of the oscillations $T_i < T_{res}$, Figure 9b;
3. $T_i$ is exactly equal to the period of the voltage oscillations $T_{res} = 1/f_{res}$, Figure 9c.

Figure 9. Illustration of PDN voltage variations in Time Domain and Victim timing variations:
a) PDN transient response on a single transition; b) PDN voltage at 10 consecutive aggressor current pulses; c) PDN voltage at aggressor current pulses “match” the period of the oscillations.
In a first case the PDN voltage oscillations will decay after each transition and the waveform presented on Figure 9a will repeat at each of the aggressor transition; as one can see from the Figure 9a, in this case PDN voltage oscillations might reach a very high value.

In the second case, when aggressor is repeating faster compared to the oscillations period, the PDN voltage after first aggressor transition starts rising, but is knocked down by next aggressor transition, then rising again, etc. After 10 pulses, as considered on Figure 9b the voltage also oscillates and then is stabilized at the value that is equal to the supply voltage. However, if aggressor transitions will continue, the PDN voltage after decay time will not experience big variations, but exhibits a reduced value: voltage on the die rails will be less compared to the supply voltage.

In the third case two consecutive aggressor transitions correspond to the half of a period of the system oscillations that provide the maximum voltage variations in the PDN, Figure 9c. This is also worse case from the point of PDN voltage variations. Note that it becomes possible to explain all these specifics using TD analysis; these specific could not be revealed with the Frequency Domain approach.

### 7.2. On-chip Victim Timing variations

The knowledge of the PDN transient response helps to explain the timing relationships between aggressor transitions and system voltage oscillations. However, the Victim timing depends also on Victim relative position in time respect to the PDN voltage variations.

In the first case presented on Figure 9a, Victim timing might not be affected if victims’ edges positions correspond to the moments when voltage in the PDN equal to its undisturbed value before aggressor transition – before 10ns on Figure 9a. So, victim timing might not be affected, while PDN voltage experience significant variations. Otherwise, victim timing will be impacted strongly if some victim edges positions will correspond to the maximums of the PDN voltage waveform, other group of victim edges corresponds to minimums of a voltage waveform, and third group of edges has a position before the aggressor transition.

In the second case, when aggressor was silent and then starts switching frequently, like on Figure 9b, there are significant victim timing variations observed after starting the aggressor activity. For the synchronous aggressor and victim case there will be also Jitter dependence of phase between aggressor and victim.

In a third case that corresponds to the voltage variations on Figure 9c, when victim’ two consecutive pulses positions correspond: first, to the voltage drop and second, to the moment when PDN voltage reaches the maximum, there will be strong victim timing variations. The lower graph on Figure 9c demonstrates the movement of the victim edges. The arrows show the direction of the pulses movement: at voltage drop, the victim pulse is pulled out and at peak of the PDN voltage, the victim pulse is pulled in.

So, there are many different situations possible depending on aggressor and victim relative positions and system resonance frequency; we considered just some simple examples that demonstrate the behavior of victim timing at non-periodic aggressor.

### 8. On-chip Jitter and advanced Technologies

When CMOS technology advanced to the 90-, 65-, 40-, and 28-nm nodes, it enabled the higher speed products. At higher speed the products power consumption rose and on-die current variations also became stronger. The last one, together with reduced devices’ transition time cause increased voltage variations on power rails inside the chip at switching logic due to system parasitic inductance \( L \). Using next simple equation
\[ \Delta V_{PDN}(t) = L \cdot (dI(t)/dt) \] one could estimate voltage variations inside high speed devices and is astonishing that it might easily reach about 40\% - 50\% of a nominal power voltage. For these reasons the development of high speed nm-devices meets significant troubles associated with internal interaction of different chip digital components through common power supply or ground return pass. In the industry, significant attention was paid to these problems: from the development EDA Tools for the PDN voltage variations analysis to embedding special measurement devices into the chip, as it is described in [17].

As it follows from previous analysis and experiments, the main cause of the on-chip signals Jitter is a chip Dynamic current variation due to toggling internal chip logic. Some methods were developed for the reduction of the chip’ Dynamic current variations: using additional blocks inserted into the chip to compensate the current variations [5, 19]. In [20] the phase between Data and Clock Tree was optimized to reduce PDN noise. Effective way to reduce on-chip current variations is implementation of the CML type CMOS logic. This type of the logic has significantly reduced current fluctuations.

The last solution is implementing in SiGe on CMOS technology, which also is using a CML design in a SiGe part of a chip. This dual technology allows to combine the high speed device’ blocks fabricated with SiGe and CMOS logic in one piece of silicon. The example of an output waveform of a Multiplexer [21] designed for 100 Gb/s Telecom Optical communication equipment is shown on Figure 10. The Multiplexer receives 10 channels, plus the SFI-S deskew channel at 11.32 Gb/s, and outputs four lanes at 28.3 Gb/s, with a maximum output voltage of 1.2 Vpp differential. The important advantage of SiGe on CMOS technology is also a low noise of the SiGe that helps to achieve low devices Jitter. Therefore, the integrated random rms jitter for this device was 185 fs and deterministic jitter was less than 4.7 ps [21], and measured bit-error rates for the Multiplexer and Demultiplexer in a full loop - back configuration was better than 10^{-15}. The Multiplexer is a one of two devices described in [21] fabricated with IBM’s SiGe 130 nm 8HP process (210 GHz ft).

![Figure 10. Eye diagram of one of 4 outputs Multiplexer fabricated with dual SiGe and CMOS technology [21] running at 28.3 Gb/s without pre-emphasis, at nominal voltage and 80^\circ C.](image)

What is important for this paper study is that SiGe part of devices using CML design that practically excludes the Dynamic current variations at logic switching: the current just “redistributed” from one branch of a logic element to another branch, leaving the total current flow from the power supply almost constant. The reduced current variations results on reduced devices on-chip Jitter and, consequently, low BER. However, the requirements for the Serdes devices targeted 100 Gb/s and 40 Gb/s Telecom Optical equipment have also increased. This calls for the deeper on-chip Jitter analysis in a CML logic which is a subject for another paper.
9. Conclusions

We researched on-die internal signals Jitter induced through common PDN by toggling on-chip logic. The effect of a doubling Aggressor frequency impacting the Victim’ timing was introduced. The Aggressor and Victim frequencies relationships are presented which correspond to the max and min Aggressor impact to the Victim. Base on noted frequencies relationships, the method for measurement of the worse case victim Jitter inside the chip was developed for periodic aggressor and victim cases. The method does not require embedding into the IC measurement devices, significantly reduces the time required for the on-chip jitter evaluation, and might be implemented for evaluation jitter inside any chip. The practical measurements revealed a jitter resonance in a system of Chip-Package-PCB-Decoupling capacitors. Using this method on-chip Jitter studied in Frequency, Time, Spatial Domains, and versus Decoupling. It is demonstrated that the common approach to the reducing PDN noise by increasing the decoupling on PCB does not help to remove jitter resonance peak. Otherwise, lowering the PCB impedance by adding more capacitances makes the situation even worse; the value of the peak increases.

The most complex case studied is the PDN voltage variations for the non-stationary or non-periodic aggressor. For the analysis the Time Domain approach was used where the PDN resonance frequencies preliminary defined with introduced measurement method. The PDN resonance frequencies for this research might be also obtained from the simulation Tools available on the market. The examples of the simulation of noise in a PDN and behavior of on-chip internal signals jitter at non-periodic aggressor were presented. Many of the revealed specific of the PDN voltage variations, as well as victim jitter, could not be explained with using frequency Domain approach.

Using theory and methods described in this paper one can evaluate on-chip Jitter using a stationary periodic aggressor, define system resonances, evaluate PDN voltage variations and predict on-chip Victim Jitter behavior for the non-stationary aggressor. Using the obtained results, it is possible to improve device performance by reducing or avoiding increased fluctuations in a system of Chip-Package-PCB-Decoupling.

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