

PROTECTION PRODUCTS

Gigabit Ethernet Protection

As the volume of network traffic increases, the industry moved quickly from 10Base-T to 100Base-T (Fast Ethernet). Yet the growth of complex computing applications moves the industry to Gigabit Ethernet for an even higher speed network technology at the backbone and server level. Eventually Gigabit Ethernet will migrate to desktop for general applications. Gigabit Ethernet has four types of physical layer signaling: 1000Base-SX (short wavelength optical fiber), 1000Base-LX (long wavelength fiber), 1000Base-CX (short run copper) and 1000Base-T (100-meter, four pair category 5 UTP). 1000Base-T is often the more favored solution for many networks because of its lower cost-of-entry.

Transient Threats

1000Base-T operates at 125 MHz clock and transmits and receives (full duplex) on four twisted pairs. It uses a bi-directional five-level coding scheme that requires a complex PHY chip. 1000Base-T PHY chips are routinely manufactured using 0.18-micron technology with some using 0.13-micron technology. These small geometries are sensitive to fatal electrostatic discharges that may originate from a charged cable, lightning or a "human body". One of the most common electrostatic discharges is a Cable Discharge Event (CDE). A CDE occurs when an Ethernet cable becomes charged (due to its environment) and subsequently discharges into the circuit when the cable is plugged into the connector. In general, the waveforms last for a few hundred nanoseconds with rapid polarity changes. Another frequent phenomenon is human "thumping" of the connectors of the cable resulting in an immediate ESD event. These types of waveforms last for approximately 60ns and are consistent with the human body model as defined by immunity standards such as IEC 61000-4-2. For outside connections, lightning can also induce high voltage onto the lines that can be transferred to the Ethernet PHY IC. These events are high energy pulses, lasting several microseconds. Many systems supporting 1000 Base-T are required to meet the IEC61000-4-2 (ESD) if it is an inside line and IEC61000-4-5 level 2 (lightning) if it is an outside line.

Ethernet ports are highly susceptible to line-to-line or metallic surges. During a metallic surge, current will flow into one line, through the transformer and back to

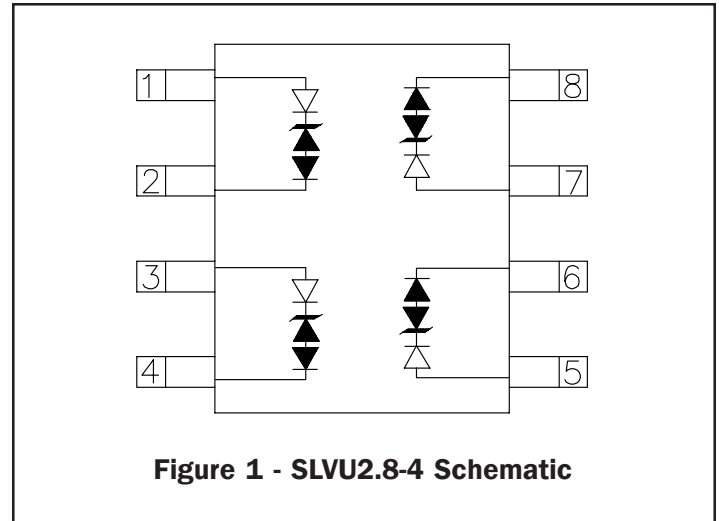


Figure 1 - SLVU2.8-4 Schematic

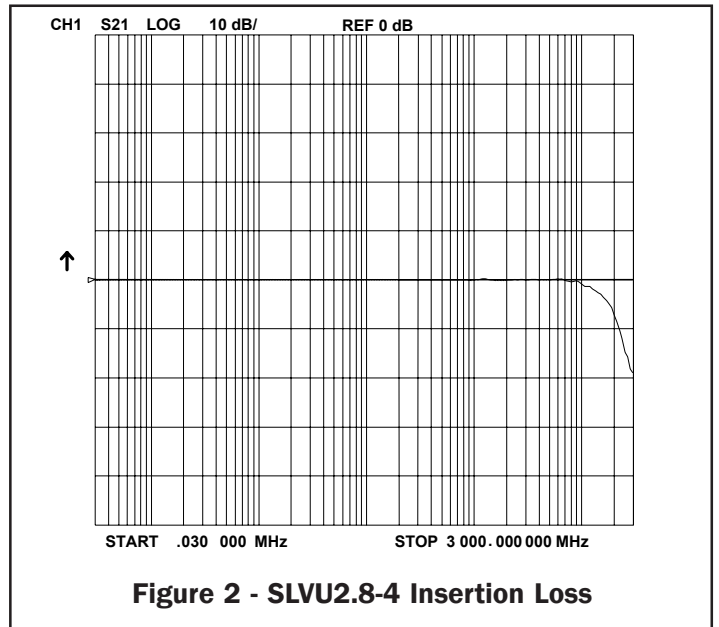


Figure 2 - SLVU2.8-4 Insertion Loss

the source. As the current flows, it charges the secondary windings of the transformer. Once the surge is removed, the secondary winding will stop charging and will transfer its stored energy to the primary side where the PHY IC is located. Internal protection circuitry of Ethernet PHY chips is limited at best. It often consists of small rail-to-rail diodes or thick epi layers to increase the immunity of the device. Often the internal protection circuit is damaged during the initial discharge followed by damage to the CMOS structure after subsequent discharges. Catastrophic failures are easy to detect and identify. Latent failures are however very difficult to find and often manifest themselves as "bugs" and reliability problems.

PROTECTION PRODUCTS**Protecting Gigabit Ethernet Ports**

Transient protection of a Gigabit Ethernet interface can be challenging. The high-speed data transmission requires the protection device to have low capacitance to prevent signal degradation and low clamping voltage to reduce stress on the protected IC. Semtech's SLVU2.8-4 meets these criteria. The circuit diagram of SLVU2.8-4 is shown in Figure 1. It is in a SO-8 package and may be used to protect two high-speed line pairs. The TVS diode is constructed using a proprietary EPD process technology yielding a device with superior electrical characteristics at an operating voltage of 2.8V. The series compensation diode acts to reduce the loading capacitance to a maximum of <8pF per line. The "flow-thru" design minimizes trace inductance and reduces voltage overshoot associated with ESD events. Combined with low leakage current, this means signal integrity is preserved. A typical insertion loss curve is shown in Figure 2. As shown, there is virtually no loss to 1GHz. The SLVU2.8-4 is designed to meet the transient immunity standards of IEC 61000-4-2, level 4 (ESD – 15kV air and 8kV contact), IEC 61000 – 4-4, level 4 EFT and IEC61000-4-5 level 2 (Lightning 24A 8/20 μs) as referenced by ETSI EN 300 386.

Figure 3 shows how to configure two SLVU2.8-4's to protect all four twisted pairs (8 lines) on the Gigabit Ethernet port. Note that the traces are run through the device since the lines are not internally connected in the SLVU2.8-4. In this configuration the SLVU2.8-4's provide bi-directional differential mode protection for

positive and negative surges. Pins 1 and 8 are connected to one line of a twisted pair while pins 2 and 7 are connected to the other line of that same twisted pair. Pins 3 and 6 are connected to one line of another twisted pair while pins 4 and 5 are connected to the other line of that same twisted pair. During a transient event, the SLVU2.8-4 will turn on and shunt the current away from the transformer and back to the source. The low clamping voltage of the SLVU2.8-4 also minimizes the stress on the protected IC. Transformer isolation of at least 1.5kV is usually sufficient for common mode protection. Capacitors (C1 – C8) provide additional common mode protection. The common mode protection can be further enhanced by adding Semtech's SRV05-4 RailClamp to the IC side of the circuit. These devices add approximately 3pF of loading capacitance and will clamp the line voltage to a diode drop above the supply voltage.

Board Layout Considerations For ESD Protection

Board layout plays an important role in the suppression of extremely fast rise-time ESD transients. Recall that the voltage developed across an inductive load is proportional to the time rate of change of current through the load ($V = L di/dt$). The total clamping voltage seen by the protected load will be the sum of the TVS clamping voltage and the voltage due to the parasitic inductance ($V_{c(TOT)} = V_c + L di/dt$). *Parasitic inductance in the protection path can result in significant voltage overshoot, reducing the effectiveness of the suppression circuit.*

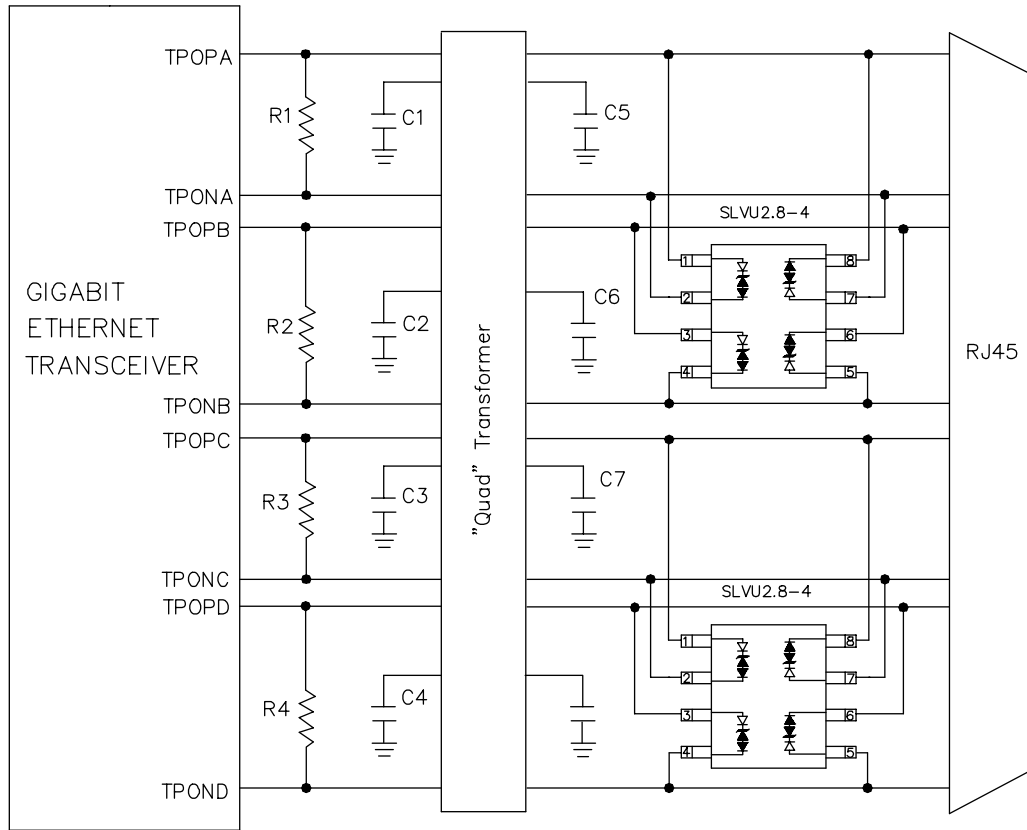


Figure 3 - Gigabit Ethernet Protection Circuit