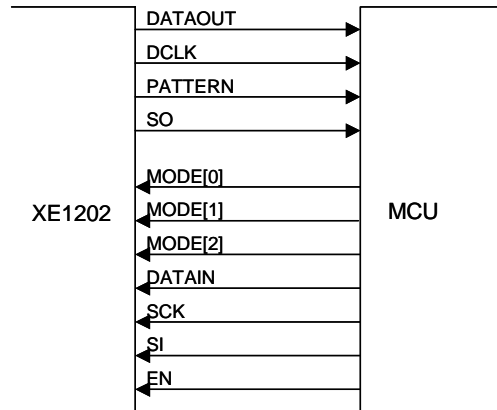

TN1200.03

Technical Note

***Interfacing the XE1202
to a Microcontroller***

INTRODUCTION

The XE1202 device is defined with 11 interface lines from a baseband processor or MCU; DATAOUT, DATAOUT, and DCLK - data and data clock, PATTERN - the output of the pattern recognition feature, SCK, SI, and SO for the 3-wire serial bus interface, MODE[2:0] to define the operating mode, and EN which operates as a chip select line. 4 lines are outputs, 7 are inputs.

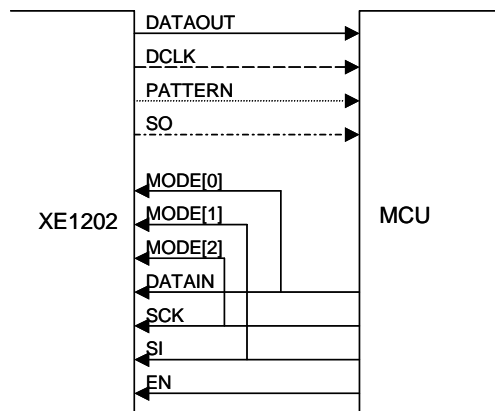


Some applications may require less I/O lines and/or fewer features. In this case and under well-defined conditions it is possible to reduce the number of lines between an MCU and the XE1202.

MINIMUM INTERFACE WITHOUT ADDITIONAL CIRCUITRY

For applications that do not require the bit synchronizer output DCK¹, nor the pattern recognition, nor the RSSI and FEI functions, it is possible to reduce the number of lines down to 5 without additional circuitry. This is achieved by multiplexing MODE[2:0] with SCK, SI, and DATAIN. One additional line is required for each of the features listed above (DCK, PATTERN, and SO for the RSSI/FEI). This is illustrated in the figure below.

Note¹:this doesn't imply the bit synchronizer function is OFF. One can turn this function ON and use it as a data filter on DATAOUT

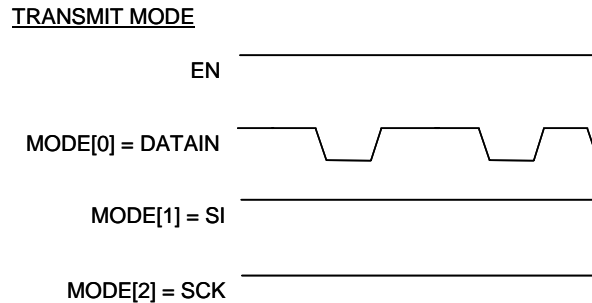


The multiplex of MODE[2:0] with SCK, SI, and DATAIN implies some careful design to avoid difficulties with XE1202, as listed on the next page.

STANDARD OPERATING MODE

When in sleep, stand-by, receive, or transmit mode, EN, SI = MODE[1], and SCK = MODE[2] should stay “high”.

In transmit mode DATAIN = MODE[0] will vary according to the bit stream to be emitted while in transmit mode. Otherwise this line can be “high” or “low”.

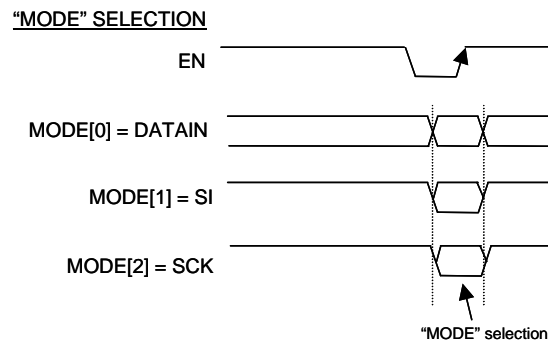


MODE Selection

To modify the MODE selection one should proceed as follows:

- the EN line becomes “low”
- then the new MODE selection is applied to MODE[2]=SCK, MODE[1]=SI, and MODE[0]=DATAIN. Here, it is key to limit the number of transitions on MODE[2]=SCK to less than 8 (in principle none or one should be sufficient)
- then the EN line becomes “high”
- finally, the SCK and SI go back to “high” and DATAIN back to the level it had before the MODE selection.

This is illustrated below

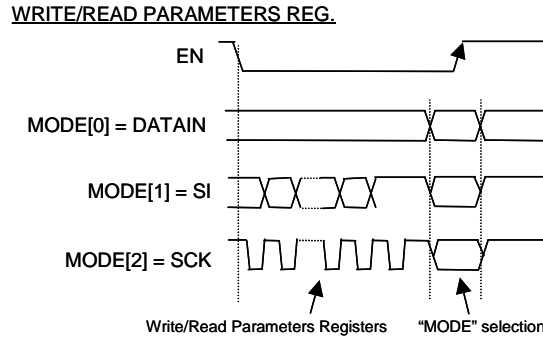


Write/Read to/from the parameters registers

Here, user should first follow the standard write or read sequence described in the xe1202 datasheet. As described in this document, while the EN line is “low” it is possible to write in one or more registers. These sequences must be complete sequences with the appropriate number of clock cycles on SCK.

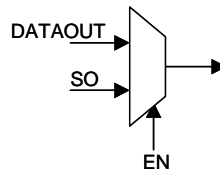
Then, and before the EN line is set to “1”, the MODE selection should be applied to MODE[2]=SCK, MODE[1]=SI, and MODE[0]=DATAIN. Here, it is key to limit the number of transitions on MODE[2]=SCK to less than 8 (in principle none or one should be sufficient)

After this the EN line goes “high”, and finally SCK and SI go back to “high” and DATAIN back to the level it had before the MODE selection.



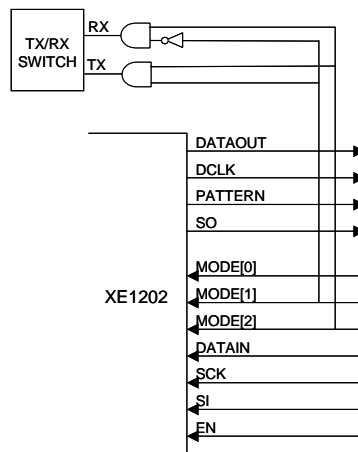
MINIMUM INTERFACE WITH ADDITIONAL CIRCUITRY

Further to the multiplex of input lines listed above, it is possible to combine both DATAOUT and SO lines through a MUX that is controlled by the EN line. When in normal operating mode (EN=1), DATAOUT is selected, while in write/read parameters registers mode (EN=0) SO is selected. By doing so, it is assumed the incoming bitstream on DATAOUT can be ignored while the XE1202 is accessed through its 3-wire serial bus interface.



TX/RX SWITCH CONTROL

For applications that require a Tx/Rx switch in the transmit/receive path between the antenna and XE1202, the control circuitry below is recommended.



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Contact Information

Semtech Corporation
Wireless and Sensing Products Division
200 Flynn Road, Camarillo, CA 93012
Phone (805) 498-2111 Fax : (805) 498-3804