
TN1202.02

Technical Note

XE1202 Basic Settings

1. INTRODUCTION

This document provides some guidance for the settings of the XE1202 UHF transceiver for the basic mode of operation. These different parameters are programmable through the 3-wire serial bus interface into the different configuration registers.

2. FREQUENCY DEVIATION, BASEBAND FILTER BANDWIDTH VS. BITRATE AND REFERENCE CRYSTAL TOLERANCE

The bit rate, the frequency deviation and the baseband filter bandwidth of XE1202 are programmable through the serial bus interface. However, these parameters are not independent and there are several rules to comply with to ensure a successful operation.

Before addressing the different settings, let's investigate the Local Oscillator frequency error topic.

2.1 Local Oscillator Frequency Error

First, let's define Δf_{LO} as the actual frequency error of the local oscillator compared to the desired value. Similarly, Δf_{RF} is the actual frequency error of the received carrier frequency compared to the desired value.

The accuracy of the LO depends on the reference crystal frequency error. The errors on that frequency are the manufacturing tolerance at the reference temperature $\Delta fs(0)$, the stability over temperature range $\Delta fs(\Delta T)$, and aging $\Delta fs(\Delta t)$. Other mechanisms can create additional errors, such as shocks, but they are not considered here. Over the operating temperature range and over time, the maximum frequency error is the sum of these 3 components: $\max. \Delta f_{LO} = \Delta fs = \Delta fs(0) + \Delta fs(\Delta T) + \Delta fs(\Delta t)$ [ppm]. This LO drift combined with the carrier frequency error Δf_{RF} affects the behavior of the demodulator, which in turn affects the achievable sensitivity. It can also affect the Frequency Error Indicator (FEI) function of XE1202.

The LO frequency error can be compensated by various techniques such as trimming during manufacturing, having an AFC algorithm - which can be facilitated by the FEI function -, having a sensor for temperature compensation.

2.2 Demodulator: LO Frequency Error vs. Frequency Deviation

The direct conversion architecture of XE1202 and the structure of its demodulator are such that the frequency error f_{offset} due to Δf_{RF} and Δf_{LO} must be lower than 40% of the frequency deviation.

$$f_{offset} = | \Delta f_{RF} - \Delta f_{LO} | < 0.4 * \text{Frequency deviation}$$

Beyond this value, one will see loss of sensitivity. Then, the receiver won't be able to operate.

2.3 Setting The Frequency Deviation vs. Desired Bitrate

These parameters are controlled by the FSParam_Dev and FSParam_BR internal registers. The selected frequency deviation (expressed in Hz) must be greater or equal to the desired bitrate (expressed in bits/s). This results in a modulation index larger or equal to 2 which is necessary to guarantee correct functioning of the demodulator and bit synchronizer.

$$\text{Frequency deviation} \geq \text{Bit rate}$$

Combining these 2 conditions leads to a limited set of frequency deviation depending on the desired bitrate and shows the maximum frequency error at the demodulator input. This is summarized below.

Bitrate (NRZ) [bits/s]	Frequency Deviation [Hz]	Max frequency error f_{offset} [ppm]*		Baseband filter BW (ssb) [Hz]	Comment
		[Hz]	*for 915 MHz operation		
4800	5000	2000	2	10000	
4800	10000	4000	4	20000	
4800	20000	8000	9	40000	
4800	40000	16000	17	200000	
4800	100000	40000	44	200000	
9600	10000	4000	4	20000	
9600	20000	8000	9	40000	
9600	40000	16000	17	200000	
9600	100000	40000	44	200000	
19200	20000	8000	9	40000	
19200	40000	16000	17	200000	
19200	100000	40000	44	200000	
38400	40000	16000	17	200000	
38400	100000	40000	44	200000	
76800	100000	40000	44	200000	

The 4th column from the right hand side indicates the maximum error in [ppm] for operation in the 902 – 928 MHz band.

The first conclusion at this stage is that for applications/products without any type of LO compensation – no trimming, no temperature compensation, no pairing – the maximum frequency error Δf_s of the reference crystal should be consistent with the maximum error frequency f_{offset} shown in the table above. Two cases should be considered:

- a) Similar XE1202-based transceivers are used on both end of the communication link. The worst case condition is when the frequency errors on both ends add up, for example when the 2 crystals are mismatched and the terminals operate at very different temperatures. In this case both Δf_{RF} and Δf_{LO} contribute to f_{offset} , so Δf_s should be better than half of the value shown above. For example, for a 915 MHz system using 100kHz frequency deviation, the tolerance and stability of the reference crystal over the operating temperature range should be better than 22 ppm. Or in other words, with a 10ppm tolerance/10ppm stability crystal, the recommended setting for frequency deviation is 100 kHz.
- b) One side of the communication link has a precise local oscillator. In this case one can assume only Δf_{LO} contributes to f_{offset} , so Δf_s should be better than the value shown in the table above. For example, for a 915 MHz system using 40kHz frequency deviation, the tolerance and stability of the reference crystal over the operating temperature range should be better than 17 ppm. Or, with a 20ppm tolerance/20ppm stability crystal, the recommended setting for frequency deviation is 100 kHz.

If trimming or pairing, which will reduced $\Delta f_s(0)$, is used during UHF board manufacturing, then a reference crystal with looser stability can be used as long as the condition above is verified. For example, a system operating at 915 MHz with 20ppm tolerance/20ppm stability crystal on both ends of the communication link can be used with 100 kHz deviation if both units are trimmed to the desired frequency at the reference temperature.

The baseband filter bandwidth should be programmed in register RTParam_BW as indicated in the table above.

2.4 Setting The Baseband Filter Bandwidth VS. Desired Bitrate

As indicated above the very fine resolution of the XE1202 frequency synthesizer can be used to efficiently compensate the LO frequency error without additional external components. This is achieved by adding the necessary frequency offset to the desired carrier frequency when programming the frequency synthesizer in the FSParam_Freq registers.

One can estimate the frequency error $|\Delta f_{RF} - \Delta f_{LO}|$ using the FEI feature of XE1202. Compensating for this error allows the use of reference crystal with looser tolerance compared to the examples above. However, there are some constraints to operating the FEI when setting the frequency deviation and baseband filter bandwidth. To guarantee a proper behavior of the FEI the sum of frequency offset and the signal bandwidth (ssb) should be lower than the baseband filter bandwidth (single sided). That is

$$|\Delta f_{RF} - \Delta f_{LO}| + \text{SignalBW} < \text{Baseband_filterBW}$$

A fair approximation of the modulated signal bandwidth (single sided) is equal to the sum of the bitrate divided by 2 and the frequency deviation (Bitrate/2 + Frequency Deviation).

This leads to the possible settings summarized below

Bitrate (NRZ) [bits/s]	Frequency Deviation [Hz]	Signal BW (ssb) [Hz]	Baseband filter BW (ssb) [Hz]	Maximum frequency offset [ppm]*		Comment
				[Hz]	*for 915 MHz operation	
4800	5000	7400	10000	2600	3	
4800	5000	7400	20000	12600	14	
4800	5000	7400	40000	32600	36	
4800	5000	7400	200000	192600	210	
4800	10000	12400	20000	7600	8	
4800	10000	12400	40000	27600	30	
4800	10000	12400	200000	187600	205	
4800	20000	22400	40000	17600	19	
4800	20000	22400	200000	177600	194	
4800	40000	42400	200000	157600	172	
4800	100000	102400	200000	97600	107	
9600	10000	14800	20000	5200	6	
9600	10000	14800	40000	25200	28	
9600	10000	14800	200000	185200	202	
9600	20000	24800	40000	15200	17	
9600	20000	24800	200000	175200	191	
9600	40000	44800	200000	155200	170	
9600	100000	104800	200000	95200	104	
19200	20000	29600	40000	10400	11	
19200	20000	29600	200000	170400	186	
19200	40000	49600	200000	150400	164	
19200	100000	109600	200000	90400	99	
38400	40000	59200	200000	140800	154	
38400	100000	119200	200000	80800	88	
76800	100000	138400	200000	61600	67	

This table shows that reference crystal can have looser tolerance/stability compared to the non-compensated case. How loose depends on the other compensation techniques in the system. Without other compensation – no trimming, no pairing, no temperature sensor – control algorithms with the FEI can be simple or sophisticated, depending on the system/application constraints. For the very basic cases it is recommended to set the desired bitrate and frequency deviation first and then to set the filter bandwidth according to the crystal tolerance/stability. More sophisticated algorithms can include a second tuning step.

Again, if trimming or pairing, which will reduced $\Delta f_s(0)$, is used during UHF board manufacturing, then smaller baseband filter bandwidth or reference crystal with looser stability can be used as long as the condition above is verified.

3. Configuration And Status Registers

XE1202 has a series of configuration registers programmable through the serial control interface. Their name, size, address and description are listed in the table below. The size of these registers is 1, 2, 3, or 4 bytes. Their byte address is a 5 bit address, A[4:0].

Name	Size	Reg Address	Description
RTParam	2 x 8 bit	00000 00001	Receiver and transmitter parameters registers
FSParam	3 x 8 bit	00010 00011 00100	Frequency parameters
DataOut	1 x 8 bit	00101	Transceiver data register
ADParam	2 x 8 bit	00110 00111	Additional parameters
Pattern	4 x 8 bit	01000 01001 01010 01011	Reference pattern for the "pattern recognition" function

In addition, 16 bytes at addresses A[4:0] = 10000 to 11111 are reserved for test purpose

Name	Size	Reg Address	Description
Test	16 x 8 bit	10000 to 11111	Reserved (test registers)

All the bits that are referred as "Reserved" in this section should be set to "0". At power-up, all registers are set to "0".

3.1 RTPARAM Configuration Register

Reg address 00000			
Name	Bits	Basic setting	Description
	7	0	
RTParam_Bits	6	1	Bit synchronizer on
RTParam_RSSI	5	0	RSSI off
RTParam_FEI	4	0	FEI off
RTParam_BW	3-2	11	200 kHz Bandwidth for the BB filter (see section 1 above)
RTParam_Tpow	1-0	00, 01, 10, or 11	0, 5, 10, or 15 dBm output power

Reg address 00001			
Name	Bits	Basic setting	Description
RTParam_Osc	7	0	Ref freq. from on-chip Xtal oscillator
	6	1	
RTParam_Filter	5	0	No pre-filtering of bit stream in transmitter mode

Reg address 00001			
Name	Bits	Basic setting	Description
RTParam_Fsel	4	1	FEI uses correlators
RTParam_Stair	3	0	Rise and fall time set to 10% bit duration (when RTParam_Filter = 1)
RTParam_Modul	2	0	Modulator turned On in transmit mode
RTParam_RSSR	1	0	Low range of the RSSI
RTParam_Clkout	0	1	Clock signal available on CLKOUT (39MHz divided by 4, 8, 16 or 32)

3.2 FSPARAM Configuration Register

Reg address 00010			
Name	Bits	Byte Address	Description
FSParam_Band	7-6	01, 10, or 11	433, 868, or 915 MHz band
FSParam_Dev	5-3	100	100 kHz frequency deviation (see section 1 above)
FSParam_BR	2-0	010 (or 000, 001, 011, 100)	19.2 kbits/s bitrate (see also section 1 above)

Name	Bits	Byte Address	Description
FSParam_Freq			434.00 MHz if this band selected
Reg address 00011	7-0	00000000	869.00 MHz “
Reg address 00100	7-0	00000000	915.00 MHz “

3.3 ADPARAM Configuration Register

Reg address 00110			
Name	Bits	Byte Address	Description
ADParam_Pattern	7	0	Pattern recognition off
ADParam_Psize	6-5	10	24-bit data for pattern recognition (for example)
ADParam_Ptol	4-3	01	1 error admitted for pattern recognition (for example)
ADParam_Clkfreq	2-1	00	1.22 MHz on CLKOUT
ADParam_IQA	0	0	IQ amplifiers off

Reg address 00111			
Name	Bits	Byte Address	Description
ADParam_Res1	7	0	
ADParam_Invert	6	0	Non inverted data on DOUT
ADParam_RegBW	5	0	Automatic regulation of the bandwidth of the base-band filter
ADParam_Regfreq	4	0	Regulation of the bandwidth of the base-band filter upon receiver start-up
ADParam_Regcond	3	0	Regulation process of the base-band filter bandwidth restarted each time the bandwidth is modified
ADParam_WBBcond	2	0	Boosting process of the base-band filter restarted each time the bandwidth is modified
ADParam_Xsel	1	0	Ref Xtal with CL + C0 = 15 pF
ADParam_Res2	0	0	

3.4 Pattern Register

Name	Bits	Byte Address	Description
Pattern			
Reg. Address 01000	7-0	01010101	(This is a simple example to detect preamble)
Reg. Address 01001		01010101	
Reg. Address 01010		01010101	
Reg. Address 01011		01010101	

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