Surge Protection of ISDN S/T-Interfaces

This application note describes how to implement transient surge protection for ISDN S/T-interfaces. The protection technique shown is suitable for use in NT and TE equipment including PC-based ISDN adaptor cards.

ISDN S/T-interface equipment may be exposed to transient voltages from a variety of sources including electrostatic discharge (ESD) and lightning. With exposure of the S/T-interface bus to these transient voltages, supplemental protection components are necessary to protect the terminal equipment from damage or reliability degradation.

Protection may be implemented on the line side or device side of the transformer. Although line side protection has less of an impact on impedance templates, it is more expensive than device side protection schemes. Device side protection may have a greater impact on impedance template margins due to capacitance multiplication by the transformer. Due to the nature of the transient stresses expected at S/T-interfaces, line side surge protection is normally not necessary.

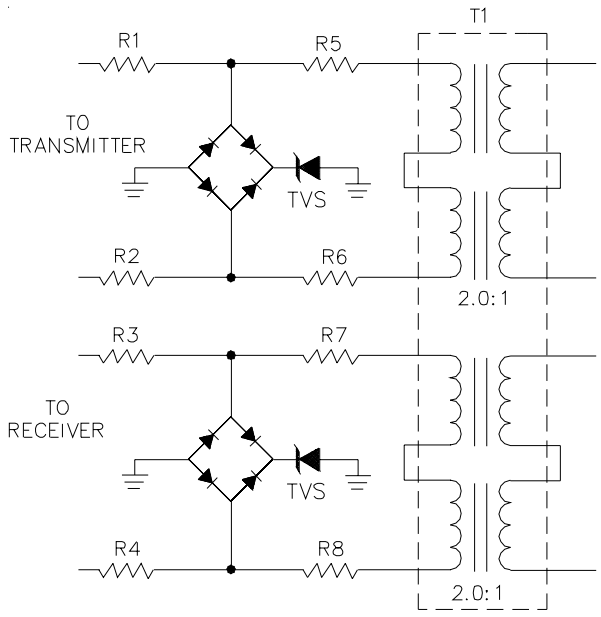

Figure 1 -Enhanced Diode Bridge Protection Circuit

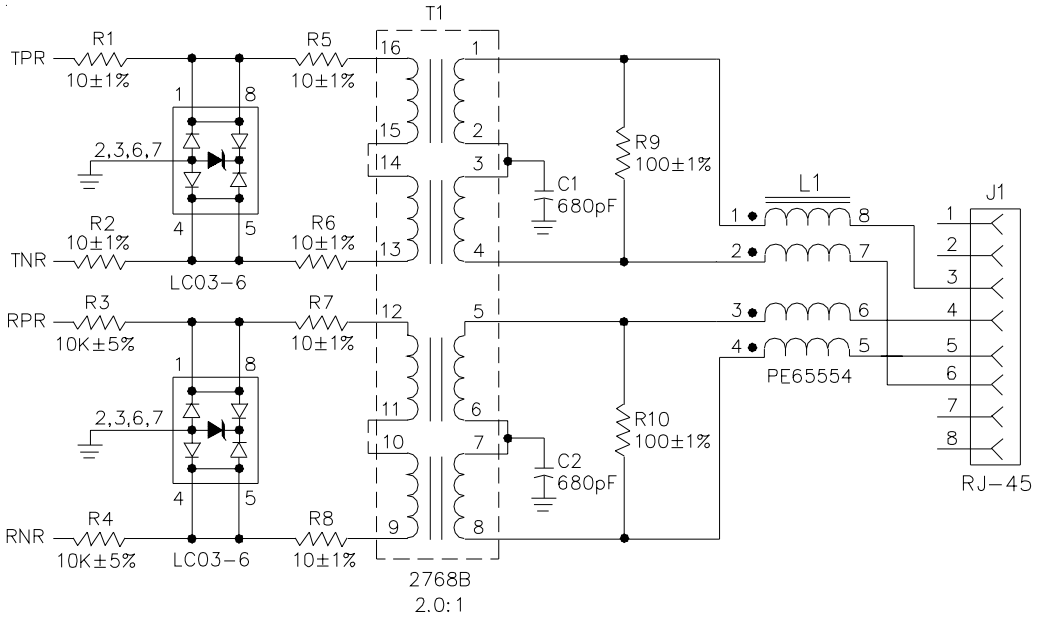

Figure 2 - ISDN S/T-Interface Circuit With Surge Protection

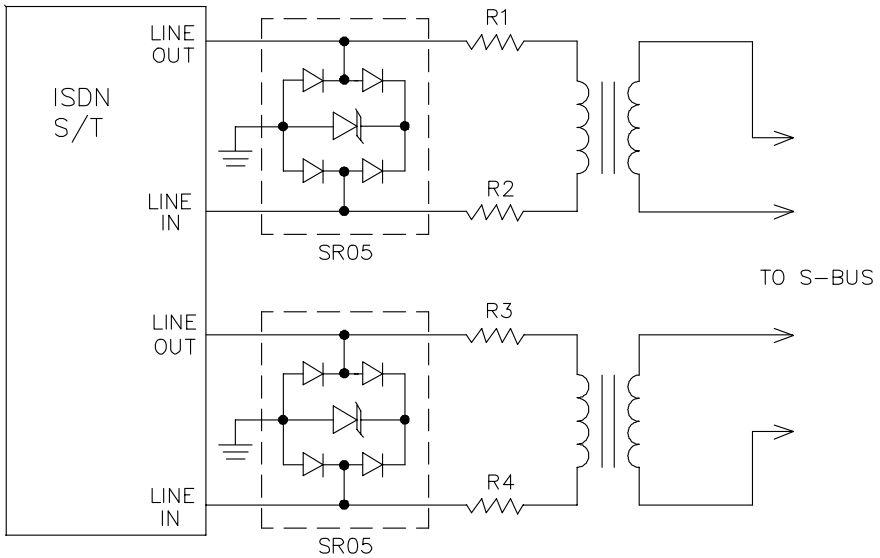

Figure 3 - Alternative Protection Circuit

The device side protection scheme should have the following characteristics:

- High surge capability
- Ability to handle multiple surges without damage
- Low capacitance
- Attenuate surges in common and differential mode
- Low clamping and operating voltage
- Fast response time

Often, the enhanced diode bridge design is used for surge protection (Figure 1). The bridge rectifiers are used as steering diodes to route the incoming surge safely through the TVS diode. Implementation with discrete components can be tricky however. First, selection of the bridge diodes is critical. The selected devices must have high forward surge capability and extremely fast switching times to be effective against ESD and lightning induced surges. Second, device layout is critical in order to reduce overshoot voltages associated with trace inductance. Finally, high component count can cause design problems when pc board space is at a premium.

The Semtech LC03-6 is an alternate solution to discrete components. The LC03-6 is specifically designed to meet the criteria necessary for protection on ISDN and other high speed interfaces. The LC03-6 contains the diode bridge and high power TVS diode within a single device. A complete S/T-interface design example is shown in Figure 2. The LC03-6 is implemented on the device side of the line transformer across each transmit and receive line pair. The lines run through the device at pins 1 & 8 and 4 & 5. Pins 2, 3, 6, and 7 provide the ground connection path. When connected in this manner, the LC03-6 will protect the transceiver IC from differential and common mode surges. The device begins to clamp at 6.8V, well below the breakdown voltage of the transceiver's internal diodes. The transceiver series line resistors (R1 - R8) are split and the LC03-6 is placed at the splitting point. This provides current limiting for the LC03-6 as well as the transceiver IC. Some typical resistor values are shown in Figure 2. The exact values of the resistors depends upon the transceiver requirements and transformer characteristics, and will vary depending upon the application. The transformer center tap capacitors C1 and C2 are used for EMI suppression. Again, actual values will vary depending upon specific applications and system requirements. R9 & R10 are line termination resistors. The above design is suitable for meeting most transient immunity standards including Bellcore 1089 (intra-building) and ITUK.20. For applications with less stringent surge requirements, the SR05 may be used as the primary protection element (Figure 3). The device is configured in a low capacitance bridge configuration and will suppress transient resulting from electrostatic discharge (ESD) and tertiary lightning. As always, to ensure compliance with all regulatory requirements, completed designs should undergo the necessary testing at an approved lab for design verification.