

POWER MANAGEMENT**Description**

The SC458 is a single chip high-performance PWM controller designed to power advanced processors. On-chip support is provided for Active Voltage Positioning, "VID on-the-fly" transitions, single and dual phase control.

The SC458 implements hysteretic control technology which provides the fastest possible transient response while avoiding the stability issues inherent to classical PWM controllers. Semtech's proprietary Combi-Sense® technology provides a loss-less current sensing scheme which is extremely robust and easy to lay out. Eliminating the sense resistors reduces costs and PCB area, plus increases system efficiency. Integrated SmartDriver™ technology initially turns on the high side driver with 'soft' drive to reduce ringing, EMI, and capacitive turn-on of the low side MOSFET, while also increasing overall efficiency.

Hysteretic operation adaptively reduces the SC458 switching frequency at light loads. Combined with an automatic "power-save" mode which prevents negative current flow in the low-side FET, system efficiency is significantly enhanced during light loading conditions. The SC458 changes from dual-phase to single-phase operation whenever DUAL transitions low, providing optimal efficiency across the entire power range. A second low power control pin, DRIFT, allows the output voltage to be discharged by the load during a negative voltage transition.

A 7-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements a 0.300V to 1.500V range. The DAC slew rate is externally programmed to minimize transient currents and audible noise. True differential remote sensing provides accurate point-of-load regulation at the processor die. Other features include programmable soft-start, dual (delayed, and not delayed) power good outputs, dynamic current sharing, over voltage and programmable over current protection. The SC458 is available in a space- saving 44 pin MLP package.

Features

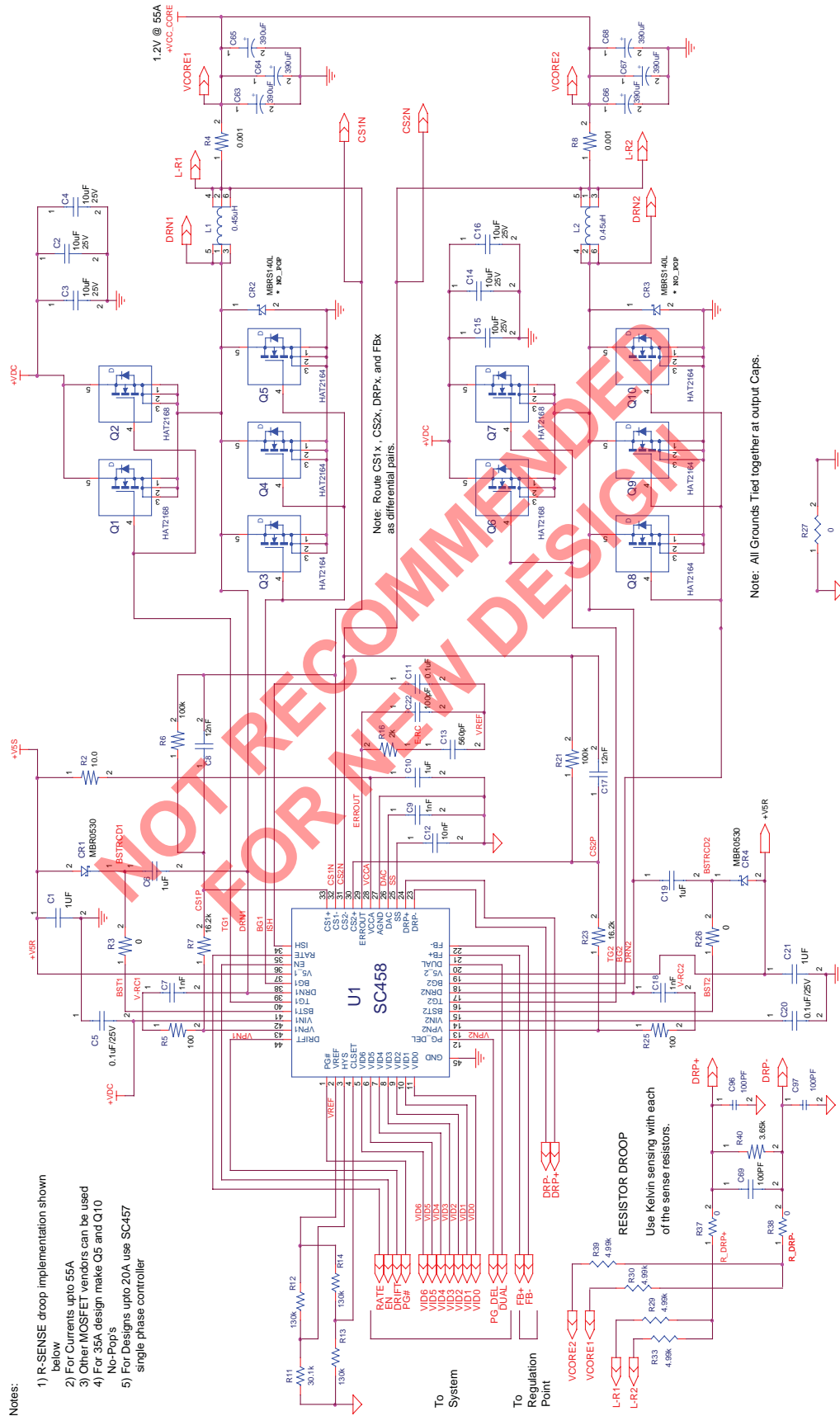
- ◆ Dual-Phase Solution with Integrated Drivers
- ◆ Hysteretic Control for Fast Transient Response
- ◆ Combi-Sense Loss-Less Current Sensing
- ◆ Dynamic Current Sharing
- ◆ Active Voltage Positioning
- ◆ True Differential Remote Sensing
- ◆ Dual Power Good Outputs
- ◆ Programmable Soft-Start and DAC Slew Control
- ◆ Programmable OCP Threshold
- ◆ Supports all Ceramic Decoupling Solutions
- ◆ 44 pin MLP (7x7 mm)
- ◆ Product is WEEE and RoHS Compliant

Applications

- ◆ Graphics and other Processor Cores
- ◆ Notebook PCs
- ◆ Embedded Applications

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Typical Application Circuit



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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Condition	Min	Max	Units
Supply Voltages VCCA V5_1, V5_2		-0.3	6.5	V
BST1, BST2 to PGND	Static	-0.3	30	V
	Transient < 100ns	-0.3	34	V
BST1, BST2 to DRN1, DRN2		-0.3	6	V
DRN1, DRN2 to PGND	Static	-2	25	V
	Transient < 100ns	-5	29	V
TG1, TG2 to PGND		DRN 1, 2-0.3	BST1, 2+0.3	V
BG1, BG2 to PGND		-0.3	V5_1, 2+0.3	V
VIN1, VIN2 to PGND		-0.3	25	V
VPN1, VPN2 to PGND		-0.3	VIN1, 2+0.3	V
PGND to AGND		-0.3	0.3	V
All other pins to AGND		-0.3	VCCA+0.3	V
Thermal Resistance Junction to Ambient ⁽¹⁾	θ_{JA}		21	°C/W
Operating Junction Temperature Range	T_J	-40	125	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Peak IR Reflow (10-40sec)	$T_{IRreflow}$		260	°C
ESD Rating (Human Body Model) ⁽²⁾	V_{ESD}	2		kV

Notes:

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad as per JESD51 standards.

(2) Tested in accordance to JEDEC standard JESD22-A114B.

Electrical Characteristics

Unless otherwise specified, VCCA = V5_1 = V5_2 = 5V, -40 < T_J < +125°C.

Parameter	Condition	Min	Typ	Max	Units
Supplies (VCCA, V5_1, V5_2)					
VCCA, V5_1, V5_2 Operating Range		4.5	5.0	5.5	V
V _{BAT} Operating Range		4.5		24	V
VCCA, V5_2 UVLO	Rising	4.25	4.4	4.5	V
	Hysteresis Falling	50	150	250	mV

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Supplies (VccA, V5_1, V5_2) (Cont.)					
VccA Current	Disabled			10	μA
	In UVLO		0.6	1.0	mA
	Operating (static)	5	10	15	
VccA Operating Current	Operating (Deeper Sleep)		8	12	mA
V5_1 Current	Disabled			10	μA
	In UVLO			10	
	Operating (Static, TG1 Low)	0.3	0.9	1.2	mA
V5_2 Current	Disabled			10	μA
	In ULVO		120	200	
	Operating (Static, TG2 Low)	0.3	0.9	1.2	mA
Vin1 and Vin2 Current	Static TG when respective TG low		500		μA
	Static TG when respective TG High		900		
	When in Powersave		0		
Logic Inputs (EN, VID[6:0], DRIFT, DUAL)					
Enable Threshold		0.8		2.0	V
VID[6:0], DRIFT, DUAL Threshold		0.45		0.65	V
Input Impedance			40		kΩ
Reference (DAC, SS, VREF) (0 < T_j < 85°C)					
DAC Error + Internal Offset	1.5000V - 0.7625V	-0.85		+0.85	%
	0.75V - 0.50V	-7		7	mV
	0.4875 - 0.30V	-14		14	
DAC Sink/Source Ability	0.3V < DAC < 1.5V	50			μA
SS Slew Current	Start-Up	8	12	16	μA
	Operating	102	120	138	
	Discharge (SS = 0.5V)	15			mA

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Reference (DAC, SS, VREF) (0 < T_J < 85°C) (Cont.)					
SS Discharge Threshold			50	100	mV
Boot Voltage		1.176	1.200	1.224	V
Boot Delay ⁽¹⁾		10	30	100	us
VREF Accuracy		1.97	2.00	2.03	V
VREF Sink/Source Ability		1.5			mA
Remote Sense (FB+, FB-)					
Input Impedance			14		kΩ
Bandwidth ⁽¹⁾		2			MHz
Droop (DRP+, DRP-)					
Input Bias Current				±1	μA
Gain	DRP+ = 1.5V, DRP- = 1.48V	9.5	10	10.5	V/V
Droop Input Offset	(25°C only)	-0.4	0	0.4	mV
	0 to -85°C	-0.5	0	0.5	
Maximum Input Common Mode Voltage		1.5			V
Maximum Input Signal		20			mV
Bandwidth ⁽¹⁾		0.8			MHz
Error Amplifier (ERROUT)					
Gain ⁽¹⁾			19		
Bandwidth ⁽¹⁾		2			MHz
Current Sensing (CS1+, CS1-, CS2+, CS2-, ISH)					
CS1, 2+, CS1, 2 Bias Currents	CS+ = CS- = 1.5V			±1	μA
CS Gain for Switching		5.4	6.0	6.6	V/V
Maximum Input Signal ⁽¹⁾		450			mV
CS Bandwidth ⁽¹⁾		2			MHz

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Current Sensing (CS1+, CS1-, CS2+, CS2-, ISH) (Cont.)					
Zero-Crossing Detector Offset		-6		6	mV
Low Pass Filter Corner Frequency ⁽¹⁾		50	80	125	kHz
Current Sharing Open Loop Gain		40	60	90	
Current Share Range		52	80	108	%
Current Sharing Offset		-3.0		+3.0	mV
Current Sharing Disable Threshold Relative to VccA	Voltage on ISH Pin	-0.9		-0.35	V
Hysteresis Setting (HYS, CLSET)					
HYS, CLSET Input Bias Current				I500I	nA
HYS Error (Internal HYS difference from TG HI to TG LO as a percentage of voltage applied at HYS pin)	HYS = 1V Dual Phase	-18	-20	-22	%
	HYS = 1V Single Phase	-24	40	-16	
CLSET Voltage (Internal hysteresis setting relative to voltage applied at CLSET pin) CLSET = 1.2V	TG High	160	200	240	mV
	TG Low	128	160	192	
	Single hase TG Low	90	120	150	
Power Good (PG#, PG-DEL)					
Leakage	PG#, PG-DEL High Impedance			1	μA
On-Resistance	PG#, PG-DEL = 0.1V			100	
PG-DEL Start-Up Delay		3.0	6.5	10	ms
Fixed Over-Voltage Protection Threshold		1.75	1.8	1.85	V
Power Good Window Upper Threshold	FB Rising Relative DAC	+160	+200	+240	mV
Power Good Window Lower Threshold	FB Falling Relative DAC	-360	-300	-240	
Power Good Window Lower Hysteresis	FB Rising Relative DAC	30	50	00	
High-Side Driver (TG1, TG2, BST1, BST2, DRN1, DRN2)					
Peak Current ^(1,2)		1.75	2.00	2.25	A

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
High-Side Driver (TG1, TG2, BST1, BST2, DRN1, DRN2) (Cont.)					
On Resistance	R , DRN < 0.5V, 25°C	4.1	5.8	7.5	Ω
	R, DRN < 0.5V,	3.48	5.80	9.24	
	R , DRN > 0.5V, 25°C	0.9	1.3	1.7	
	R, DRN > 0.5V,	0.76	1.30	2.10	
	R, 25°C	0.42	0.60	0.78	
	R, -40 to 125°C	0.34	0.60	1.01	
Rise Time ^(1,2)	C= 3nF	17	22	27	ns
Fall Time ^(1,2)	CTG = 3nF	9	12	15	
Propagation Delay ^(1,2)	From hysteretic comparator inputs to Driver output	30	45	60	
Shoot-Thru Protection Delay ⁽¹⁾		10	20	30	
Lower Side Drive (BG1, BG2, V5_1, V5_2, PGND1, PGND2)					
Peak Current ^(1,2)		3.5	4.0	4.5	A
On-Resistance	R _{BG_UP} at 25°C	0.9	1.3	1.7	Ω
	R _{BG_UP} at -40 to 125°C	0.76	1.3	2.1	
	R _{BG_DN} at 25°C	0.35	0.5	0.65	
	R _{BG_DN} at -40 to 125°C	0.28	0.5	0.86	
Rise Time ^(1,2)	C _{BG} = 3nF	5	7	9	ns
Fall Time ^(1,2)	C _{BG} = 3nF	2.5	3.5	4.5	
VPN (VPN1, VPN2, VIN1, VIN2)					
Tri-State Leakage		-600		600	nA
On Resistance	Source	100	200	400	Ω
	Sink	100	200	400	
Propagation Delay ^(1,2)	From Hysteretic Comparator Inputs to Driver Output	30	45	60	ns

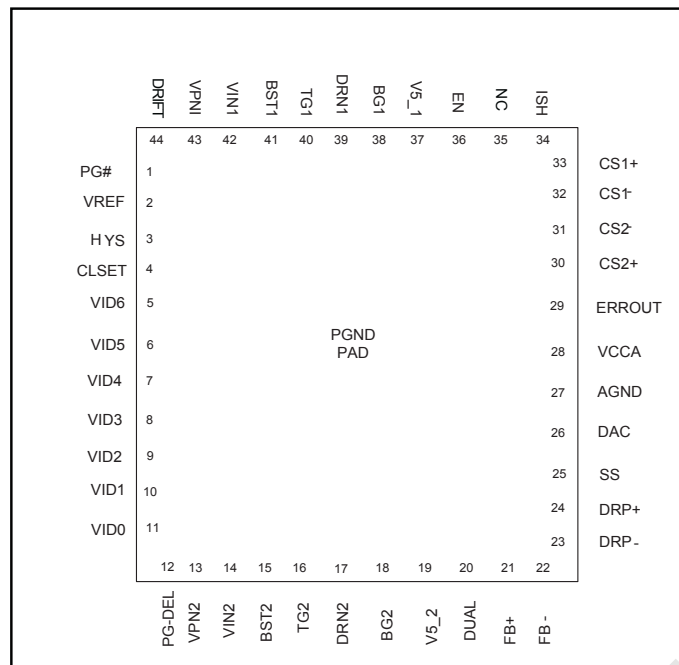
Notes:

1) Guaranteed by design.

2) T_j = 25°C.

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Pin Configuration



Ordering Information

Device ⁽¹⁾	Package ^(2,3)	Temp Range (T _J)
SC458IMLTRT	MLP-44	-40°C to +125°C

Notes:

- 1) Only available in tape and reel packaging. A reel contains 3000 devices.
- 2) This device is ESD sensitive. Use of standard ESD handling precautions is required.
- 3) Lead-free package compliant with J-STD-020B. Qualified to support maximum IR reflow temperature of 260°C for 30 seconds. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin#	Pin Name	Pin Description
1	PG#	Active low, power good, no delay - open drain output.
2	VREF	Internal reference voltage (2V). Bypass to AGND with a 1nF capacitor.
3	HYS	Core comparator hysteresis. A resistor divider on this pin sets the hysteresis voltage.
4	CLSET	Current Limit Set. A resistor divider on this pin sets the OCP threshold.
5	VID6	VID MSB.
6	VID5	
7	VID4	
8	VID3	
9	VID2	
10	VID1	
11	VID0	VID LSB.
12	PG-DEL	Active high, power good, delayed - open drain output.
13	VPN2	Virtual phase node for phase 2. Connect an RC between this pin and the output sense point to enable Combi-Sense operation.

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Pin Descriptions (Cont.)

Pin#	Pin Name	Pin Description
14	VIN2	Input power to the DC-DC converter. Used as supply reference for internal phase 2 Combi-Sense circuitry.
15	BST2	Phase 2 Bootstrap pin. A capacitor is connected between BST and DRN to develop the floating voltage for the high-side MOSFET.
16	TG2	Phase 2 output drive for the top (switching) MOSFET.
17	DRN2	This pin connects to the junction of the phase 2 switching and synchronous MOSFETs. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
18	BG2	Phase 2 output drive signal for the bottom (synchronous) MOSFET.
19	V5_2	Input supply for phase 2 low-side gate drive. Connect to 5V.
20	DUAL	Single/dual phase control. A high enables dual-phase operation. In single phase operation, the output voltage follows the DAC transition for a negative VID change.
21	FB+	Remote die sense of core voltage. Connect to VCC_SENSE at the CPU socket.
22	FB-	Remote GND sense. Connect to VSS_SENSE at the CPU socket.
23	DRP-	Inverting input to droop amplifier.
24	DRP+	Non-inverting input to droop amplifier.
25	SS	Soft-start. An external cap at this pin defines the soft-start ramp.
26	DAC	DAC output.
27	AGND	Analog ground.
28	VCCA	IC supply. Connect to 5V.
29	ERROUT	Error Amplifier Compensation Pin.
30	CS2+	Non-inverting input to phase 2 Combi-Sense amplifier.
31	CS2-	Inverting input to phase 2 Combi-Sense amplifier.
32	CS1-	Inverting input to phase 1 Combi-Sense amplifier.
33	CS1+	Non-inverting input to phase 1 Combi-Sense amplifier.
34	ISH	Used for compensation of the ISHARE amplifier.
35	NC	No connect. This pin is used internally, do not connect externally.
36	EN	Enable control. Active high.
37	V5_1	Input supply for phase 1 low-side gate drive. Connect to 5V.

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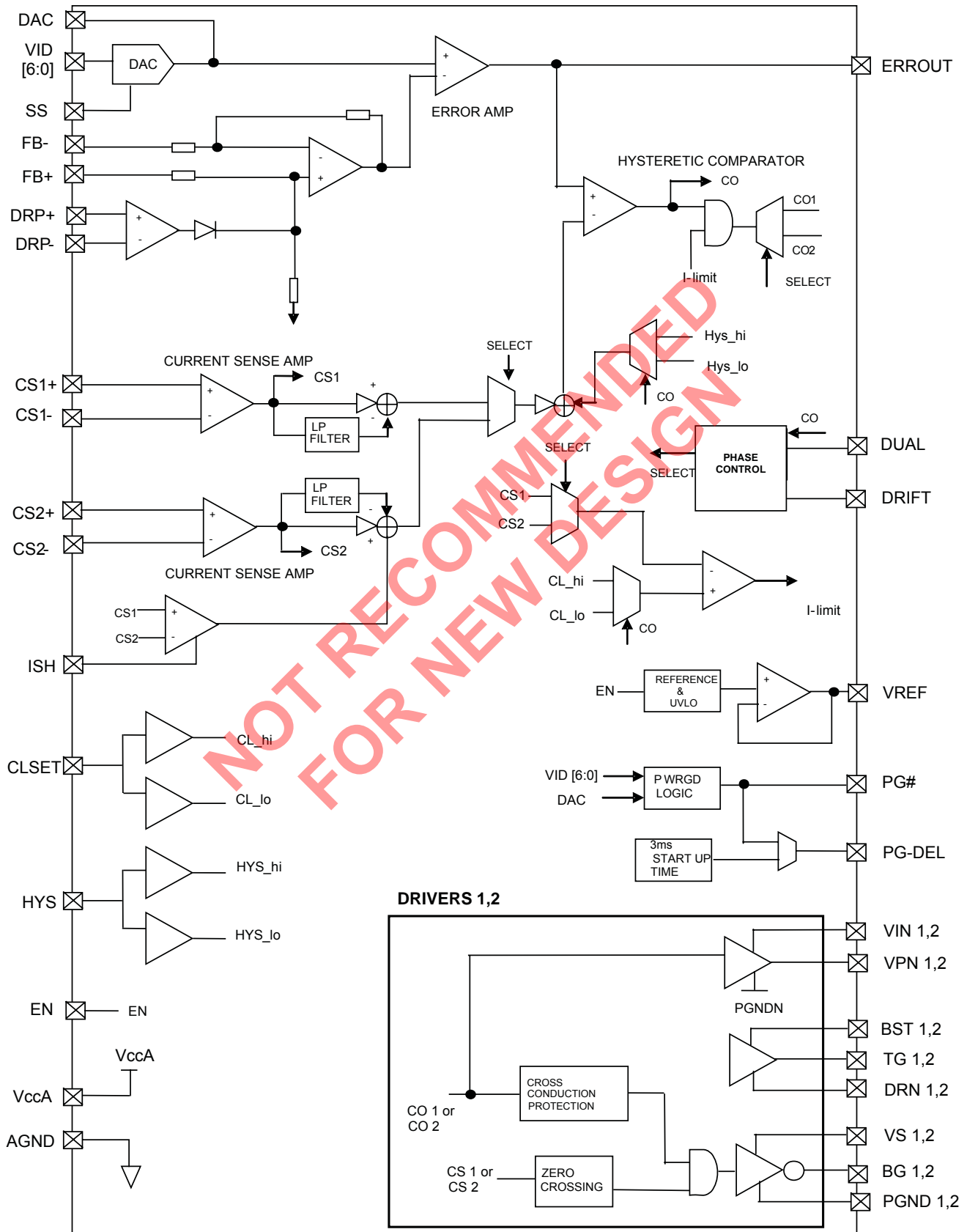
Pin Descriptions (Cont.)

Pin#	Pin Name	Pin Description
38	BG1	Phase 1 output drive signal for the bottom (synchronous) MOSFET.
39	DRN1	This pin connects to the junction of the phase 1 switching and synchronous MOSFETs. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
40	TG1	Phase 1 output drive for the top (switching) MOSFET.
41	BST1	Phase 1 Bootstrap pin. A capacitor is connected between BST and DRN to develop the floating voltage for the high-side MOSFET.
42	VIN1	Input power to the DC-DC converter. Used as supply reference for internal phase 1 Combi-Sense circuitry.
43	VPN1	Virtual phase node for phase 1. Connect an RC between this pin and the output sense point to enable Combi-Sense operation.
44	DRIFT	Second single to dual phase control. Allows output voltage to drift as a function of the load current for highest efficiency.
PAD	PGND	Power ground for drivers 1 and 2. Pad must be soldered to power ground plane.

NOT RECOMMENDED FOR NEW DESIGN

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Block Diagram



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Applications Information

Introduction

The SC458 is a new generation of hysteretic converter which combines the best features of Semtech's hysteretic converter technology with the benefits of Semtech's patented Combi-Sense technology. The SC458 provides a complete solution to processor core requirements up to and beyond 50 Adc. In the SC458, the ripple for the hysteretic switching control is provided by Combi-Sense current feedback. This provides several advantages over plain voltage-mode hysteretic converters, and other topologies such as constant-on time which switch on voltage ripple.

- No minimum amount of output ripple is required, so there are no controller-induced limits on capacitor value or ESR.
- No current sense resistors are required, resulting in higher converter efficiency.
- The large signal magnitude afforded by Combi-Sense (4-5 times that of inductor DCR current sensing) make the layout much less sensitive to noise.
- Full differential feedback of the output voltage from the CPU die is enabled.

Because the basic control is hysteretic, the SC458 provides the fastest possible transient response without switching at very high frequencies. This results in higher efficiency with less expensive parts because switching losses are reduced. Only the Combi-Sense ripple is used for the regulation loop, so the load-line accuracy is not affected by tolerances in RDS(ON) or inductor DCR. However, because of the large signal magnitude, the DC is kept for the current limiting and current sharing functions:

Load-line control is provided by a dedicated droop amplifier with uncommitted inputs. This provides users with maximum flexibility, as the droop source can be any of the following:

- PCB copper trace
- Inductor DCR
- Sense resistor

Thus, customers can choose the amount of cost and performance they need for a given design.

The SC458 also provides a full range of features. A complete suite of power management functions are implemented on-chip:

- Enable pin (EN)
- Two Power Good indicators:
 - ◆ PG#
 - ◆ PG-DEL
- Dual/Single Phase Control (DUAL)
- DRIFT pin for negative V_{OUT} transitions
- Programmable "VID-on-the-fly" support
- All 1's "soft-OFF" state
- A 2.00V voltage reference is provided
- Separate hysteresis and current limit settings.
- A full suite of protection features is provided:
 - ◆ Over-current protection (OCP)
 - ◆ Fixed and DAC-referenced over-voltage protection (OVP)
- Over-temperature protection (OTP)
- Under-voltage detection via PWRGD

All protection features are latching, and are reset either by recycling power or toggling the EN signal.

Theory of Operation

Voltage Regulation

Referring to the block diagram on the preceding page, the hysteretic comparator is the heart of the converter. The "+" input corresponds roughly to the CMPREF node of our older generations of IC; the "-" input is similar to CMP. In order to regulate, the hysteretic comparator needs the following information:

- DAC (reference) voltage
- Droop voltage proportional to I_{OUT}
- Feedback voltage
- Hysteresis voltage
- Hysteresis ripple

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Applications Information (Cont.)

Voltage Regulation (Cont.)

CMPREF receives the reference, voltage feedback and droop information. The reference is produced by the integrated seven-bit DAC. The feedback voltage is received by the full differential amplifier from the CPU socket.

The droop amplifier reduces the voltage at the “+” node of the differential amplifier as the output current increases to produce the required linear load line. A third amplifier, labeled the “Error Amplifier”, multiplies the difference between the “ideal” voltage (DAC minus droop) and the actual voltage (FB+ minus FB-) for faster response. This signal is the reference for the hysteretic comparator.

CMP has the ripple signal derived from the Combi-Sense inputs plus the hysteresis signal. The DC is stripped from the ripple signals by the combination of low-pass filter and summing amplifier. Phase two has a current sharing input derived from an averaged difference between the two phases. The ripple inputs are fed to a summer via a multiplexer which is synchronized to the active phase with the Select output. The hysteresis signal is added at the summer. The hysteresis voltage is set directly by the resistor divider from the 2V REF output.

In dual phase mode, V(hys_lo) is zero; CO of the initial phase remains low while the alternate phase is in control, so BG of the initial phase remains on through the alternate cycle, as a result, the second phase will terminate at approximately -V(hys). During single phase operation, V(hys_lo) = -V(hys).

The figure on page 14 illustrates the basic switching control. Starting with the Select line (top plot, green trace) on Phase 2, and both CO signals low. Accordingly, both bottom gate (BG) signals are on and the inductor currents in both phases are discharging as shown by the Phase 1 (orange) and Phase 2 (blue) ripple signals in the lower plot.

When CMP discharges to CMPREF, the Select line toggles, CO1 turns on, and subtracts V(hys_hi) from CMP. CO1 remains high until CMP again charges to CMPREF. Then, CO1 switches low, adding V(hys_lo) to CMP. This state is held until CMP again discharges to CMPREF. Then, the Select line toggles, CO2 turns on, and the cycle repeats.

Current Limit Regulation

In current limit, the voltage hysteretic converter is overridden by the current limit hysteretic comparator, and the TG pulse is terminated when the output of the current sense amplifier reaches the CL_hi threshold and BG is terminated at the CL_lo threshold. These thresholds are set from the CLSET resistor divider:

$$CL_hi = 0.33 * V(clset)$$

$$CL_lo = 0.20 * V(clset)$$

Current limit pulses continue until 32 pulses after the voltage droops to the PWRGD low threshold; then the controller latches off. This current limit algorithm has been used in several generations of IMVP controllers and have been proven to be extremely robust.

Start-Up and Shut-Down Sequences

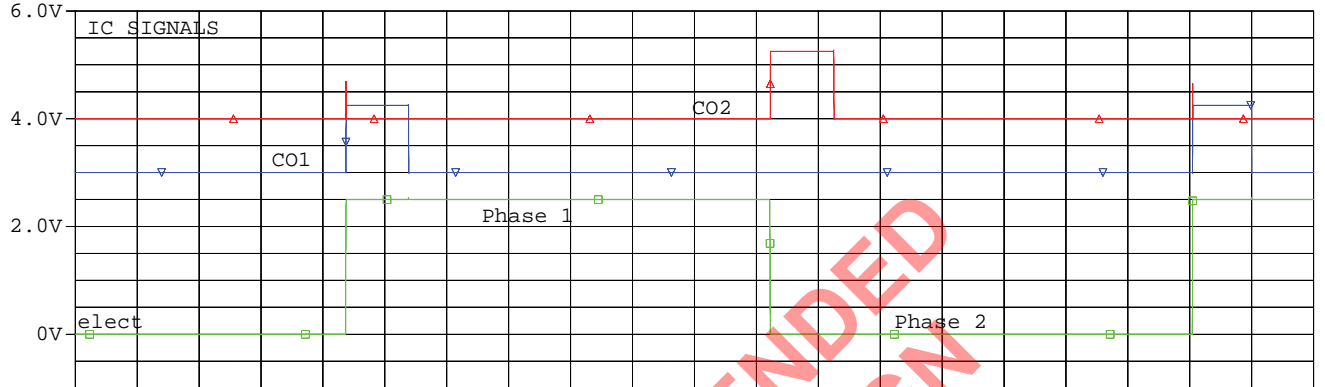
For the SC458 to start up, VCCA, V5_1, and V5_2 must reach their under-voltage lockout (UVLO) thresholds (4.4V typical). Then set the EN signal high. The DAC drives 12µA (typical) into the soft-start capacitor on the SS pin. The SS and DAC pins rise slowly until a fixed voltage (1.2V) is reached. The controller remains at this voltage for ~30µs. Then, the VID (6:0) lines are considered valid and PG# is driven low. The controller will slew at a 120µA rate to the VID-defined value. Approximately 6ms after the voltage hits the PWRGD threshold, PG-DEL goes high, and start-up is complete.

In a normal shutdown, the EN signal is driven low, the TG and BG signals are driven low, tri-stating the power chains. An approximately 50 ohm resistor on the FB+ signal discharges V_{OUT} slowly and prevents normal amounts of leakage from pulling V_{OUT} high. The DAC and other internal circuitry is shut down, entering a very low power (<10µA typical) state. An UVLO or over-current protection shutdown also results in this type of shutdown.

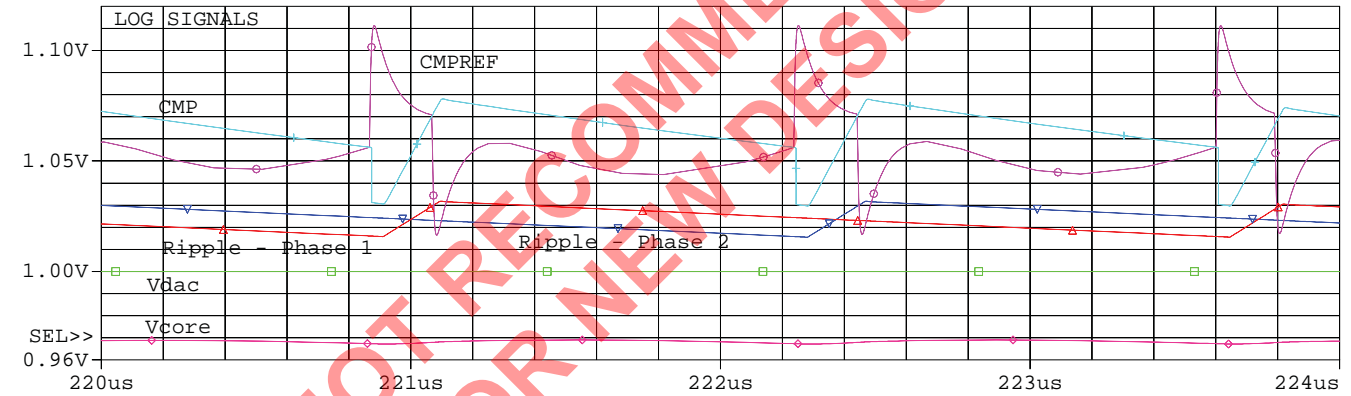
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Applications Information (Cont.)

**SC458 CBM Top Level
Temperature 27.0**



□ V(HS27.HS19:select)/2 ▽ V(HS27.CO1)/4 +3 ▲ V(HS27.CO2)/4+4



SEL>> 220us 221us 222us 223us 224us
 V(DAC) ♦ V(Vcore) ▽ V(CS2+)-V(CS2-)+1V ▲ V(CS1+)-V(CS1-)+1V ○ V(HS27.CMPREF)-0.55V
 V(HS27.CMP)-0.55V

Time

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Applications Information (Cont.)

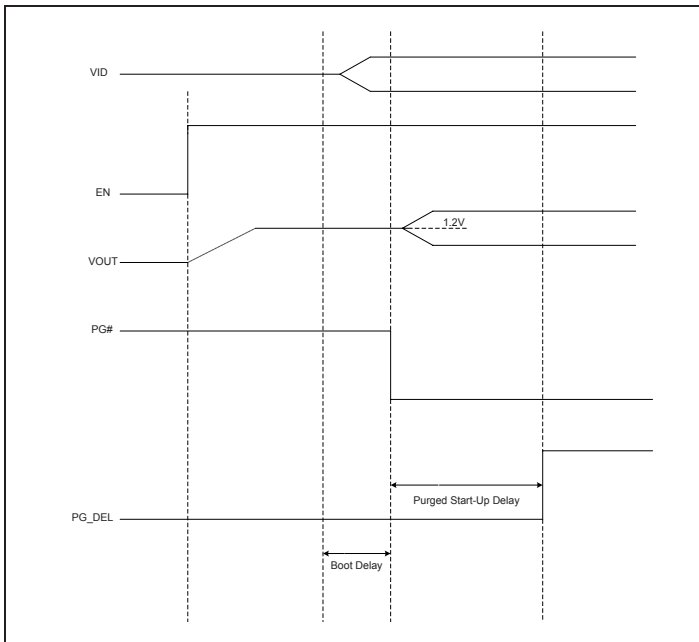


Figure 1. Power On Sequencing Timing Diagram

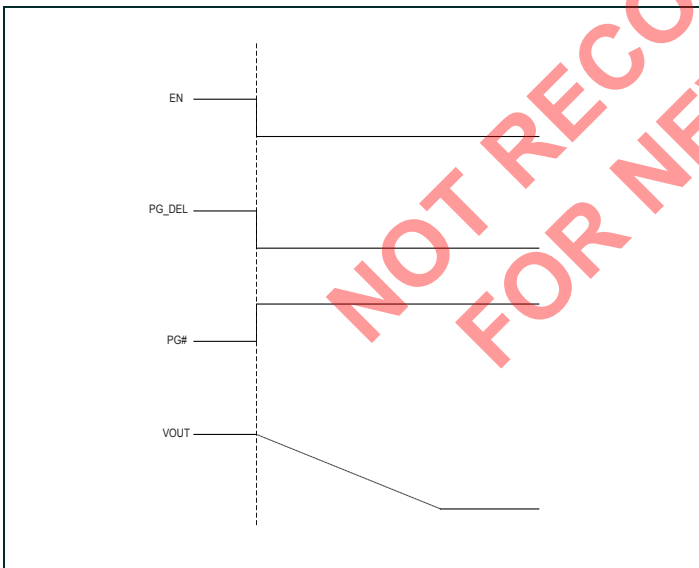


Figure 2. Power Off Sequencing Timing Diagram

DRIFT	DUAL	Supported Load	SC458 Mode	Frequency
1	0	$0 > I_{cc} > I_{MAX}/2$	1-phase	High
1	1	$0 > I_{cc} > I_{MAX}/2$	1-phase	High
0	0	$0 > I_{cc} > I_{MAX}/2$	1-phase	Normal
0	1	$0 > I_{cc} > I_{MAX}/2$	2-phase	Normal

Response to Power Control Inputs

Besides the EN signal, described above, the SC458 reacts to the other control signals in the following manner: The SC458 operates with discontinuous mode power saving enabled, always saving power at light load regardless of the status of the DUAL and DRIFT signals.

Both DUAL and DRIFT can be used to put the SC458 into single phase mode. DRIFT also reduces the hysteresis setting by 30% to increase the switching frequency at very low output voltages.

These signals allow the user to command the voltage regulator to maximize its efficiency through the widest range of output voltages and currents - from sleep to full-performance.

VID transitions are expected to be sequentially stepped (one LSB per step). The SC458 also provides controlled slewing over a larger range. In all cases, the maximum V_{OUT} slew rate is set by the size of the soft-start capacitor, as charged by the operating SS Slew Current (120µA nominal).

The SC458 recognizes a positive voltage transition and will transition to dual phase mode to supply the output bulk capacitor charge currents as well as the existing load current.

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Applications Information (Cont.)

DAC Information

A +/-0.85% 7-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. the DAC output is shown in the following table. Seven voltage identification (VID) pins are provided to support automatic selection of V_{OUT} voltages.

The DAC Voltage vs. VID [6:0] are defined in the following table. The VID [6:0] signals are have a low (0.5V) logic threshold to support low voltage CMOS drive levels. These signals also have an internal resistor to ground, so, if the VID [6:0] signals are left non-terminated, the SC458 will start up to the maximum V_{OUT} level.

DAC Operation Below 0.3000V

The SC458 responds to DAC codes corresponding to voltage values below 0.3V by producing voltages less than 0.3V; however, the tolerance of these signals is not specified or guaranteed. In the case of the '111 1111' VID code, the SC458 holds BGx and TGx low, preventing switching from occurring. In addition, a ~50Ω FET connected from V_{OUT} to GND is turned on to prevent system leakage from charging up the V_{CORE} rail.

DAC Slew Rate Control

The DAC also has integrated slew-rate control with two current settings to charge and discharge the soft-start capacitor. The slowest setting (12μA nominal) is used for soft-start, the fastest (120μA nominal) for operational voltage slewing.

Droop Amplifier

The droop amplifier provides a fixed gain of 10; as a result, only 0.3mΩ of resistance is required to produce a load-line of 3.0mV/A.

Power Supply Protection

The SC458 incorporates the full range of power supply protection circuits.

Under voltage lockout (UVLO) protection is provided on the VCCA and V5_1 inputs. This prevents problems due to inadequate control voltage or inadequate gate drive. The SC458 is in UVLO mode when its supply voltage has not ramped above the upper threshold or has dropped below the lower threshold. A UVLO condition turns off the internal bias, disables the SC458 gate drivers, and resets the soft start timer. If an UVLO occurs, the SC458 is disabled until the voltage rises above the UVLO threshold. Hysteresis is provided to prevent multiple turn-on/turn-off cycles due to ripple on these inputs.

The OVP circuit of SC458 monitors V_{OUT} for an over voltage condition. If the FB voltage is 200mV greater than the DAC-Droop (i.e. out of the power good window), the SC458 latches off and turns the low-side driver to clamp the voltage and protect the load. Either the power or EN must be recycled to clear the latch. OVP is disabled during soft-start and voltage transitions. For safety, the latch is enabled if the FB voltage exceeds 1.8V at any time.

The SC458 also incorporates thermal protection. It disables and latches off with all gate drives held low when the internal junction temperature reaches approximately 160°C. Once the IC cools by 20°C, either the power or EN must be recycled to clear the latch.

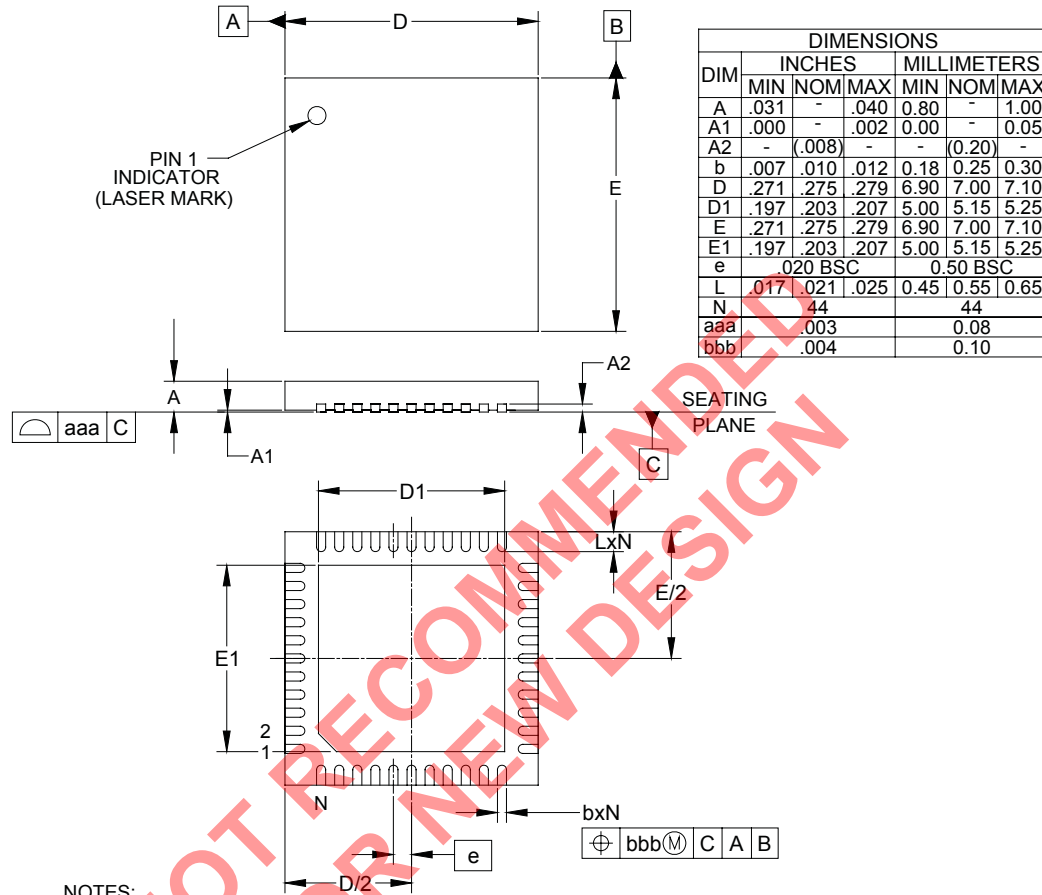
If the SC458 shuts off, use the following table to determine the type of fault.

Table 1. Fault Determination

Fault	SS Pin	REF Pin
Over-Current	Oscillates at SS rate	2V
Over-Voltage	VCCA	2V
Over-Temp	GND	2V
UVLO	GND	GND

POWER MANAGEMENT

Outline Drawing - MLP-44

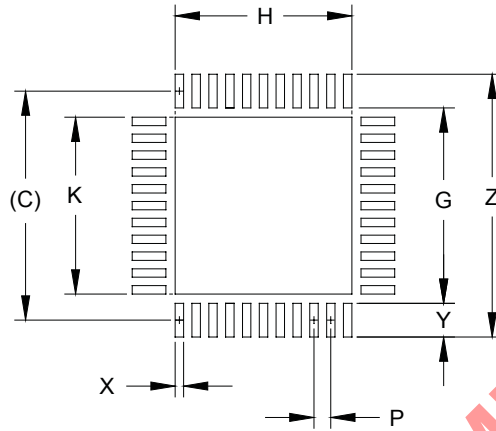


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

POWER MANAGEMENT

Land Pattern - MLP-44



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.268)	(6.80)
G	.228	5.80
H	.207	5.25
K	.207	5.25
P	.021	0.50
X	.011	0.30
Y	.039	1.00
Z	.307	7.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

NOT RECOMMENDED FOR NEW DESIGN

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