

POWER MANAGEMENT**Description**

The SC457 is a single phase, high performance PWM controller designed to power advanced processors. On-chip support is provided for VID on-the-fly transitions and active voltage positioning.

The SC457 implements hysteretic control technology providing the fastest possible transient response while avoiding the stability issues inherent to classical PWM controllers. Eliminating the sense resistors reduces costs and PCB area while increasing system efficiency. Integrated SmartDriver™ technology initially turns on the high-side driver with soft drive to reduce ringing, EMI, and capacitive turn-on of the low side MOSFET, while increasing overall efficiency.

Hysteretic operation adaptively reduces the SC457 switching frequency at light loads. Combined with an automatic power-save mode which prevents negative current flow in the low-side FET, system efficiency is significantly enhanced during light loading conditions.

A 7-bit DAC, accurate to 0.85%, sets the output voltage reference and implements the 0.300V to 1.500V range required by the processor. The DAC slew rate is externally programmed to minimize transient currents and audible noise. True differential remote sensing provides accurate point-of-load regulation at the processor die. Other features include programmable soft-start, open-drain PG_DEL and PG# outputs, dynamic current sharing, over-voltage and programmable over-current protection. The SC457 is available in a space-saving 32-pin MLP package.

Features

- ◆ Single-Phase Solution with Integrated Drivers
- ◆ Hysteretic Control for Fast Transient Response
- ◆ Active Voltage Positioning
- ◆ True Differential Remote (die) Sensing
- ◆ On-Chip Support for all Power Management Features
- ◆ Programmable Soft-Start and DAC Slew Control
- ◆ Programmable OCP Threshold
- ◆ Supports all Ceramic Decoupling Solutions
- ◆ 32-Pin MLP (5x5) - product is WEEE and RoHS compliant
- ◆ Default 1.2V Boot Voltage
- ◆ Soft OFF State

Applications

- ◆ Notebook PCs
- ◆ Embedded Applications
- ◆ Graphics and other Processor Cores

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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Parameter	Condition	Min	Max	Units
Supply Voltages VCCA, V5		-0.3	6.5	V
BST to PGND	Static	-0.3	30	
	Transient <100ns	-0.3	34	
BST to DRN		-0.3	6	
DRN to PGND	Static	-2	25	
	Transient <100ns	-5	29	
TG to PGND		DRN, -0.3	BST, +0.3	
BG to PGND		-0.3	V5, +0.3	
All Other Pins to PGND		-0.3	VCCA +0.3	
Thermal Resistance Junction to Ambient JESD51 Standard Method ⁽¹⁾	θ_{JA}		29	°C/W
Operating Junction Temperature Range	T_J	-40	125	°C
Storage Temperature Range	T_{STG}	-65	150	
Peak IR Reflow (10-40sec)	$T_{IRreflow}$		260	

Note:

1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise specified, VccA = V5 = 5V, -40° < T_J < +125°C.

Parameter	Condition	Min	Typ	Max	Units
Supplies (VCCA, V5)					
VCCA, V5 Operating Range		4.5	5.0	5.5	V
VCCA, UVLO	Rising	4.25	4.4	4.5	V
	Hysteresis Falling	50	150	250	mV
VCCA Current	Disabled			10	µA
	In UVLO		0.6	1.0	mA
	Operating (Static)	3	8	10	
V5 Current	Disabled			10	µA
	In UVLO		120	200	
	Operating, Static, TG Low	0.3	0.9	1.2	mA

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Logic Inputs (EN, VID [6:0], DRFT, RATE)					
Enable Threshold		0.8		2.0	V
VID [6:0], DRFT, RATE Threshold		0.45		0.55	
Input Impedance			40		kΩ
Reference (DAC, SS, VREF), (0 < T_j < 85°C)					
DAC Error + Internal Offset	1.5000V - 0.7625V	-0.85		+0.85	%
	0.75V - 0.50V	-7		7	mV
	0.4875 - 0.30V	-14		14	
DAC Sink/Source Ability	0.3V < DAC < 1.5V	50			μA
SS Slew Current	Start-Up	8	12	16	μA
	Operating	102	120	138	
	RATE > 0.5V & DRFT > ; 0.5V x = Operating Current	x/6	x/5	x/4	
	Discharge (SS = 0.5V)	15			mA
SS Discharge Threshold			50	400	mV
Boot Voltage		1.176	1.2	1.224	V
Boot Delay ⁽¹⁾		10	30	100	μs
VREF Accuracy		1.97	2.00	2.03	V
VREF Sink/Source Ability		1.5			mA
Remote Sense (FB+, FB-)					
Bandwidth ⁽¹⁾		2			MHz
Error Amplifier (ERROUT)					
Gain			19		
Bandwidth ⁽¹⁾		2			MHz
Current Sensing (CS+, CS-)					
CS+, CS- Input Bias Current	CS+ = CS- = 1.5V			1	μA
CS Gain - for Droop		2.7	3.0	3.3	V/V

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Current Sensing (CS+, CS-) (Cont.)					
Maximum Input Common Mode Voltage	No-Load	1.5			V
Maximum Input Signal		50			mV
Zero-Crossing Detector Threshold (Powersave)		-6		6	
Low-Pass Filter Corner Frequency ⁽¹⁾		50	80	125	kHz
Current Limit Combined System (CLSET)					
CL System Accuracy	CLSET = 1.2V, TG1 Low	28		52	mV
	CLSET = 1.2V, TG1 High	16		32	
CLSET Input Bias Current				1	μA
Hysteresis Setting (HYS)					
HYS Input Bias Current				1	μA
HYS Gain (internal hysteresis from TG low to TG high)	HYS = 1.5V	4	7	10	%
PG# (PG_DEL, PG#)					
Leakage	PG_DEL, PG# High Impedance			1	μA
On-Resistance	PG_DEL, PG# = 0.1V			100	Ω
PG# Start-Up Delay		3	6.5	10	ms
Fixed Over-Voltage Protection Threshold		1.75	1.8	1.85	V
PG# Window Upper Threshold	FB Rising Relative DAC	+160	+200	+240	mV
PG# Window Lower Threshold	FB Falling Relative DAC	-360	-300	-240	
PG# Window Lower Hysteresis	FB Rising relative DAC	30	50	70	

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Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
High-Side Driver (TG, BST, DRN)					
Peak Current ^(1,2)		1.75	2.0	2.25	A
On-Resistance	R_{TG_UP} , DRN < 0.5V, 25°C	4.1	5.8	7.5	Ω
	R_{TG_UP} , DRN < 0.5V, -40 to 125°C	3.48	5.8	9.24	
	R_{TG_UP} , DRN > 0.5V, 25°C	0.9	1.3	1.7	
	R_{TG_UP} , DRN > 0.5V, -40 to 125°C	0.76	1.3	2.1	
	R_{TG_DN} , 25°C	0.42	0.6	0.76	
	R_{TG_DN} , -40 to 125°C	0.34	0.6	1.01	
Rise Time ^(1,2)	$C_{TG} = 3nF$	17	22	27	ns
Fall Time ^(1,2)	$C_{TG} = 3nF$	9	12	15	
Propagation Delay ^(1,2)	From Hysteretic Comparator Inputs to Driver Output	30	45	60	
Shoot-through Protection Delay ⁽¹⁾		10	20	30	
Lower-Side Driver (BG, V5, PGND)					
Peak Current ^(1,2)		3.5	4.0	4.5	A
On-Resistance	R_{BG_UP} at 25°C	0.9	1.3	1.7	Ω
	R_{BG_UP} at -40° to 125°C	0.76	1.3	2.1	
	R_{BG_DN} at 25°C	0.35	0.5	0.65	
	R_{BG_DN} at -40° to 125°C	0.28	0.5	0.86	
Rise Time ^(1,2)	$C_{BG} = 3nF$	5	7	9	ns
Fall Time ^(1,2)	$C_{BG} = 3nF$	2.5	3.5	4.5	

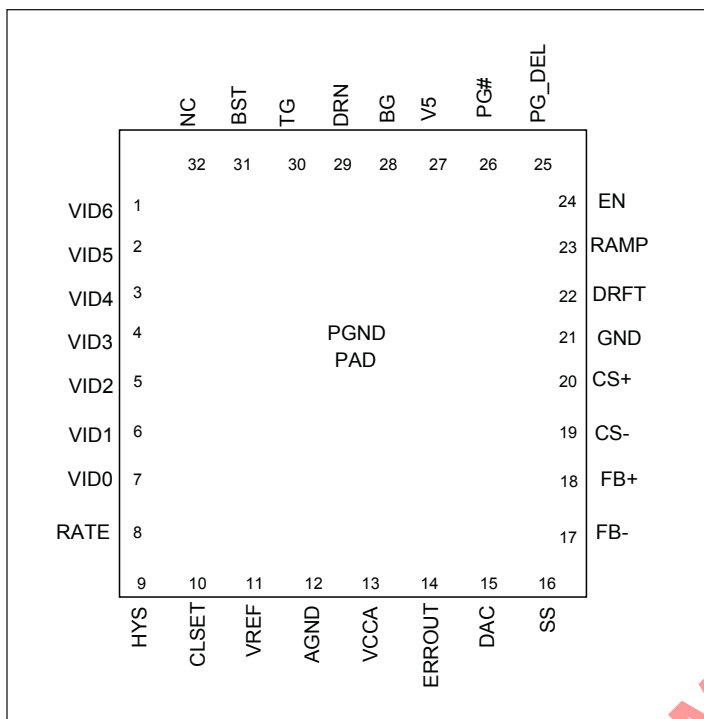
Notes:

(1) Guaranteed by design

(2) $T_j = 25^\circ C$

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Pin Configuration



Ordering Information

Device	Package	Temp Range (T _j)
SC457MLTRT	MLP-32	-40°C to + 125°C

Notes:

- 1) Only available in tape and reel packaging. A reel contains 3000 devices.
- 2) This device is ESD sensitive. Use of standard ESD handling precautions is required.
- 3) Lead-free package compliant with J-STD-020B. Qualified to support maximum IR Reflow temperature of 260°C for 30 seconds. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin#	Pin Name	Pin Description
1	VID6	VID MSB
2	VID5	
3	VID4	
4	VID3	
5	VID2	
6	VID1	
7	VID0	
8	RATE	Slew rate control pin active in DRFT mode
9	HYS	Core comparator hysteresis - a resistor divider on this pin sets the hysteresis voltage
10	CLSET	Current limit set - a resistor divider on this pin sets the OCP threshold
11	VREF	Internal reference voltage (2V) - bypass to AGND with a 1nF capacitor
12	AGND	Quiet ground for analog circuits
13	VCCA	IC supply - connect to 5V
14	ERROUT	Error Amplifier Compensation pin

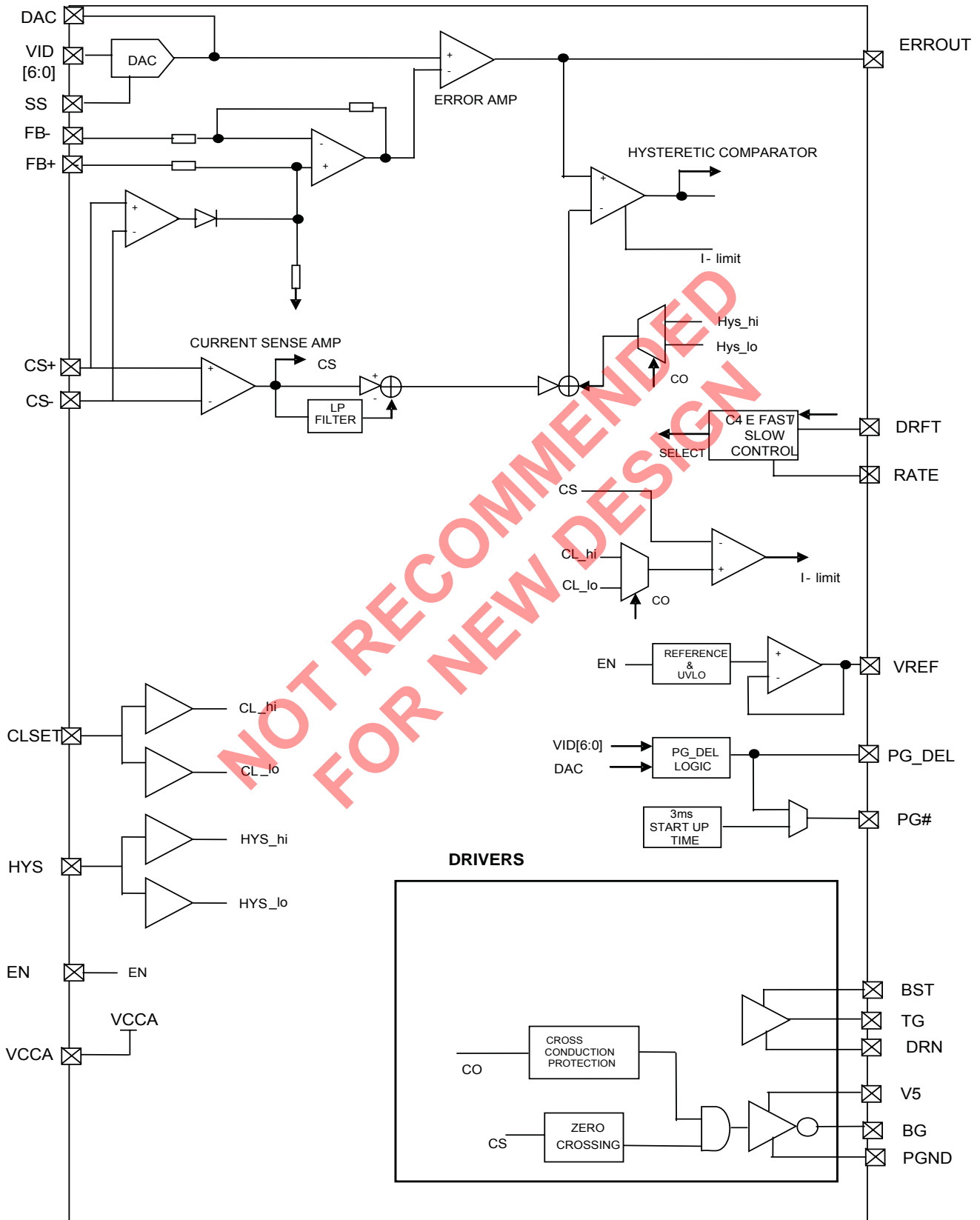
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Pin Descriptions (Cont.)

Pin#	Pin Name	Pin Description
15	DAC	DAC output - an external cap at this pin defines VID transition timing
16	SS	Soft-start - an external cap at this pin defines the soft-start ramp
17	FB-	Remote GND sense - connect to VSS_SENSE at the CPU socket
18	FB+	Remote die sense of core voltage - connect to VCC_SENSE at the CPU socket
19	CS-	Inverting input to Combi-Sense amplifier
20	CS+	Non-inverting input to Combi-Sense amplifier
21	GND	Connect to AGND
22	DRFT	DRFT mode control pin - active high
23	RAMP	An external cap defines the internal compensation ramp
24	EN	Enable control pin-active high
25	PG_DEL	Delayed power - good indicator - active high - open drain output
26	PG #	Power Good - open drain output - active low
27	V5	Input supply for low-side gate drive - connect to 5V
28	BG	Output drive for the synchronous MOSFET
29	DRN	Inductor switching node - connect to the junction of the switching and synchronous MOSFETs
30	TG	Output drive for the switching MOSFET
31	BST	Bootstrap pin - a capacitor is connected between BST and DRN to develop the floating voltage for the switching MOSFET
32	NC	No connect - leave floating
Thermal Pad	PAD	Power ground for driver

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Block Diagram



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Applications Information

INTRODUCTION:

The SC457 is a new generation of hysteretic converters which combines the best features of Semtech's hysteretic converter technology with the benefit of an error amplifier providing a complete solution.

The ripple for the hysteretic switching control is provided by DCR sensing. This provides several advantages over plain voltage-mode hysteretic converters which switch on voltage ripple.

- No current sense resistors are required, resulting in higher converter efficiency
- Full differential feedback of the output voltage from the CPU die is enabled

The SC457 provides the fastest possible transient response without switching at very high frequencies. Because the basic control is hysteretic. This results in higher efficiency with less expensive parts because switching losses are reduced.

The SC457 also provides a full range of features:

- Functions are implemented on-chip:
 - EN
 - PG_DEL
 - PG#
 - DRFT with selectable slew rates
- A 2.00V voltage reference is provided
- Separate hysteresis and current limit settings
- A full suite of protection features is provided:
 - Over-current protection (OCP)
 - Fixed and DAC-referenced over-voltage protection (OVP)
 - Over-temperature protection (OTP)
 - Under-voltage detection via PG#
 - All protection features are latching, and are reset either by recycling power or toggling the EN signal

THEORY OF OPERATION

Voltage Regulation

The hysteretic comparator is the heart of the converter (see Block Diagram on the preceding page). The "+" input corresponds roughly to the CMPREF node of our older generations of IC; the "-" input is similar to CMP.

In order to regulate, the hysteretic comparator needs the following information:

- DAC (reference) voltage
- Droop voltage proportional to I_{OUT}
- Feedback voltage
- Hysteresis voltage
- Hysteresis ripple

CMPREF receives the reference, voltage feedback, and droop information. The reference is produced by the integrated seven-bit DAC. The feedback voltage is received by the full differential amplifier from the CPU socket. The droop amplifier reduced the voltage at the "+" node of the differential amplifier as the output current increases to produce the required linear load line. A third amplifier, labeled the Error Amplifier, multiplies the difference between the ideal voltage (DAC minus droop) and the actual voltage (FB+ minus FB-) for faster response. This signal is the reference for the hysteretic comparator.

CMP has the ripple signal derived from the current sense inputs plus the hysteresis signal. The DC is stripped from the ripple signals by the combination of a low-pass filter and a summing amplifier.

Current Limit Regulation

In Current Limit, the voltage hysteretic converter is overridden by the current limit hysteretic comparator, and the TG pulse is terminated when the output of the current sense amplifier reaches the CL_hi threshold and BG is terminated at the CL_lo threshold. These thresholds are set from the CLSET resistor divider:

$$CL_hi = 0.33 * V(clset)$$

$$CL_lo = 0.20 * V(clset)$$

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Applications Information (Cont.)

Current limit pulses continue until 32 pulses after the voltage droops to the PG# low threshold; then the controller latches off. This current limit algorithm has been used in several generations of controllers and have proven to be extremely robust.

Start-Up and Shutdown Sequences

For the SC457 to start-up, VCCA, V5_1, and V5_2 must reach their under-voltage lockout (UVLO) thresholds (4.4V typical), then the EN signal goes high. The DAC drives 12µA (typical) into the soft-start capacitor on the SS pin. The SS and DAC pins rise slowly until the BOOT voltage (1.2V, fixed internally) is reached. The controller remains at BOOT voltage for ~30µs. At the end of the BOOT interval, the VID(6:0) lines are considered valid and PG_DEL is driven low. The controller will slew at a 120µA rate to the VID-defined value. Approximately 6ms after the voltage hits the PG# threshold, PG# goes high, and start-up is complete.

In a normal shutdown, the EN signal is driven low, the TG and BG signals are driven low, tri-stating the power chains. An approximately 100Ω resistor on the FB+ signal discharges Vcore slowly and prevents normal amounts of leakage from pulling Vcore high. The DAC and other internal circuitry is shut down, entering a very low power (<10µA typical) state. A UVLO will also result in this type of shutdown.

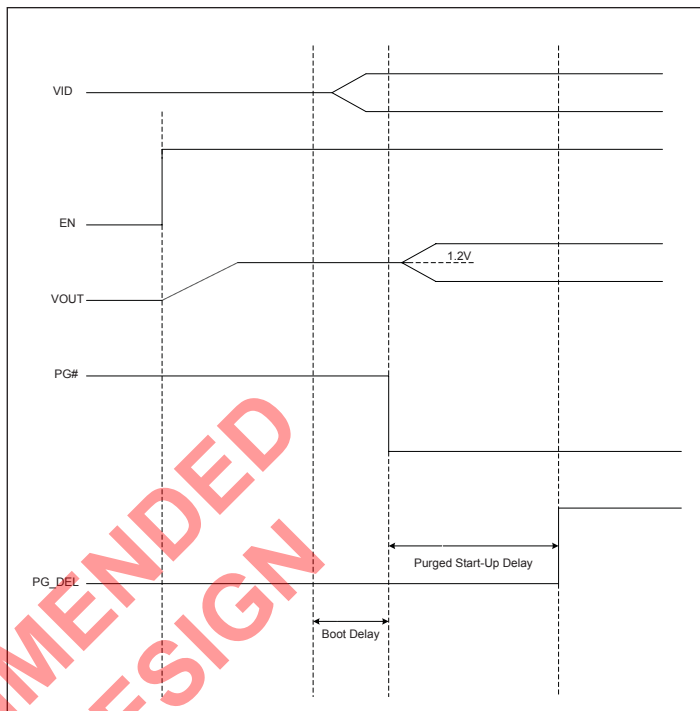


Figure 1 - Power On Sequencing Timing Diagram

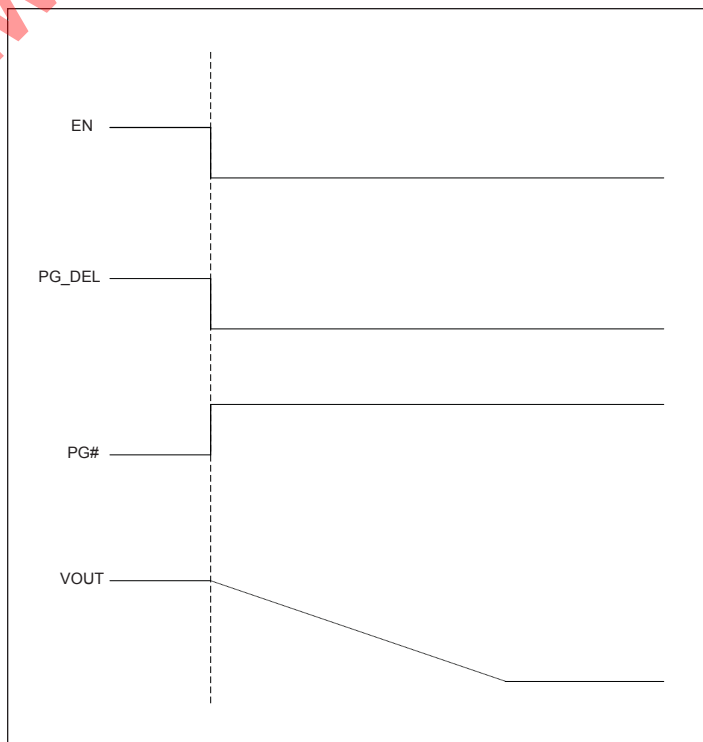


Figure 2 - Power Off Sequencing Timing Diagram

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Applications Information (Cont.)

A +/-0.85% 7-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. the DAC output

is shown in the tables below. There are seven voltage identification pins on the mobile processor. These signals can be used to support automatic selection of Vcc_core voltages.

Table 1. VID vs. DAC Voltage

VID							V _{DAC}	VID							V _{DAC}
6	5	4	3	2	1	0	V	6	5	4	3	2	1	0	V
0	0	0	0	0	0	0	1.5000	0	0	1	0	1	0	0	1.2500
0	0	0	0	0	0	1	1.4875	0	0	1	0	1	0	1	1.2375
0	0	0	0	0	1	0	1.4750	0	0	1	0	1	1	0	1.2250
0	0	0	0	0	1	1	1.4625	0	0	1	0	1	1	1	1.2125
0	0	0	0	1	0	0	1.4500	0	0	1	1	0	0	0	1.2000
0	0	0	0	1	0	1	1.4375	0	0	1	1	0	0	1	1.1875
0	0	0	0	1	1	0	1.4250	0	0	1	1	0	1	0	1.1750
0	0	0	0	1	1	1	1.4125	0	0	1	1	0	1	1	1.1625
0	0	0	1	0	0	0	1.4000	0	0	1	1	1	0	0	1.1500
0	0	0	1	0	0	1	1.3875	0	0	1	1	1	0	1	1.1375
0	0	0	1	0	1	0	1.3750	0	0	1	1	1	1	0	1.1250
0	0	0	1	0	1	1	1.3625	0	0	1	1	1	1	1	1.1125
0	0	0	1	1	0	0	1.3500	0	1	0	0	0	0	0	1.1100
0	0	0	1	1	0	1	1.3375	0	1	0	0	0	0	1	1.0875
0	0	0	1	1	1	0	1.3250	0	1	0	0	0	1	0	1.0750
0	0	0	1	1	1	1	1.3125	0	1	0	0	0	1	1	1.0625
0	0	1	0	0	0	0	1.3000	0	1	0	0	1	0	0	1.0500
0	0	1	0	0	0	1	1.2875	0	1	0	0	1	0	1	1.0375
0	0	1	0	0	1	0	1.2750	0	1	0	0	1	1	0	1.0250
0	0	1	0	0	1	1	1.2625	0	1	0	0	1	1	1	1.0125

VID							V _{DAC}	VID							V _{DAC}
6	5	4	3	2	1	0	V	6	5	4	3	2	1	0	V
0	1	0	1	0	0	0	1.0000	1	0	0	0	1	0	0	0.6500
0	1	0	1	0	0	1	0.9875	1	0	0	0	1	0	1	0.6375
0	1	0	1	0	1	0	0.9750	1	0	0	0	1	1	0	0.6250
0	1	0	1	0	1	1	0.9625	1	0	0	0	1	1	1	0.6125
0	1	0	1	1	0	0	0.9500	1	0	0	1	0	0	0	0.6000
0	1	0	1	1	0	1	0.9375	1	0	0	1	0	0	1	0.5875
0	1	0	1	1	1	1	0.9125	1	0	0	1	0	1	0	0.5750
0	1	1	0	0	0	0	0.9000	1	0	0	1	0	1	1	0.5625
0	1	1	0	0	0	1	0.8875	1	0	0	1	1	0	0	0.5500
0	1	1	0	0	1	0	0.8750	1	0	0	1	1	0	1	0.5375
0	1	1	0	0	1	1	0.8625	1	0	0	1	1	1	0	0.5250
0	1	1	0	1	0	0	0.8500	1	0	0	1	1	1	1	0.5125
0	1	1	0	1	0	1	0.8375	1	0	1	0	0	0	0	0.5000
0	1	1	0	1	1	0	0.8250	1	0	1	0	0	0	1	0.4875
0	1	1	0	1	1	1	0.8125	1	0	1	0	0	1	0	0.4750
0	1	1	1	0	0	0	0.8000	1	0	1	0	0	1	1	0.4625
0	1	1	1	0	0	1	0.7875	1	0	1	0	1	0	0	0.4500
0	1	1	1	0	1	0	0.7750	1	0	1	0	1	0	1	0.4375
0	1	1	1	0	1	1	0.7625	1	0	1	0	1	1	0	0.4125
0	1	1	1	1	0	0	0.7500	1	0	1	1	0	0	0	0.4000
0	1	1	1	1	0	1	0.7375	1	0	1	1	0	0	1	0.3875
0	1	1	1	1	1	0	0.7250	1	0	1	1	0	1	0	0.3750
0	1	1	1	1	1	1	0.7125	1	0	1	1	0	1	1	0.3625
1	0	0	0	0	0	0	0.7000	1	0	1	1	1	0	0	0.3500
1	0	0	0	0	0	1	0.6875	1	0	1	1	1	0	1	0.3375
1	0	0	0	0	1	0	0.6750	1	0	1	1	1	1	0	0.3250
1	0	0	0	0	1	1	0.6625	1	0	1	1	1	1	1	0.3125
								1	1	0	0	0	0	0	0.3000
								1	1	1	1	1	1	1	OFF

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Applications Information (Cont.)

DAC Operation Below 0.3000V

The SC457 responds to DAC codes corresponding to voltage values below 0.3V by producing voltages less than 0.3V; however, the tolerance of these signals is not specified or guaranteed. In the case of the "111 1111" VID code, the SC457 holds BG and TG preventing switching from occurring. In addition, a $\sim 50\Omega$ FET connected from V_{CORE} to GND is turned on to prevent system leakage from charging up the V_{CORE} rail.

DAC Slew Rate Control

The DAC has an integrated slew-rate control. In DRFT mode, a slower slew-rate is engaged by asserting the RATE pin. Additionally, DRFT mode allows asynchronous converter operation during voltage transitions so that the load may discharge the output capacitors as a further source of power-saving.

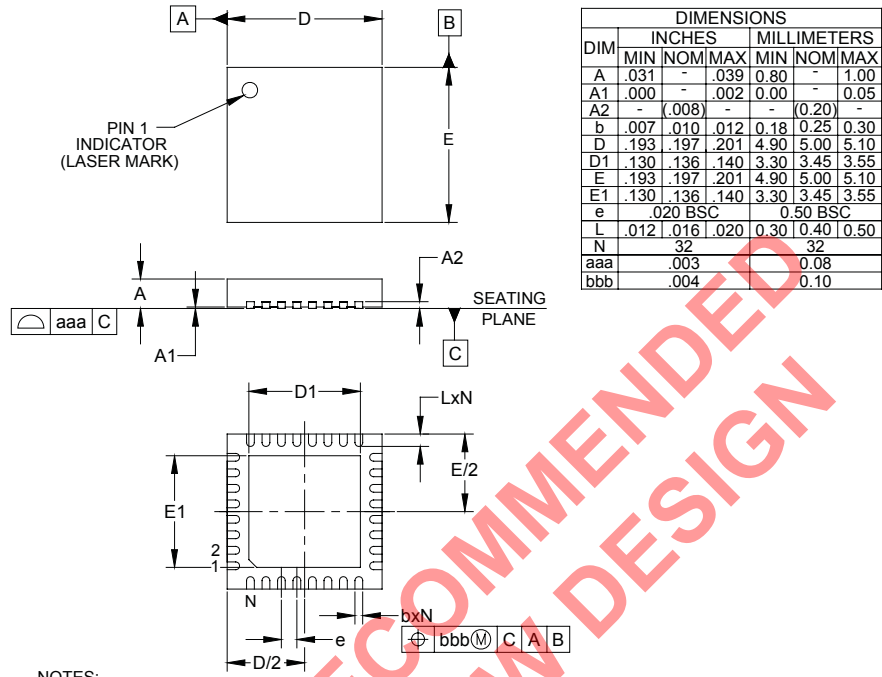
Power Supply Protection

A UVLO circuit consists of a comparator that monitors the input supply voltage level, 5V. The SC457 is in UVLO mode when its supply voltage has not ramped above the upper threshold or has dropped below the lower threshold. The output of the UVLO comparator, gated with the ENABLE signal, turns on or off the internal bias, enable or disable the SC457 output, and initiate or reset the soft-start timer.

The OVP circuit of SC457 monitors the processor core $V_{\text{CC_CORE}}$ voltage for an over-voltage condition. If the FB voltage is 200mV greater than the DAC-Droop (i.e., out of the PG# window), the SC457 will latch off and hold the low-side driver on permanently. Either the power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/DRFT transitions. For safety, the latch is enabled if the FB voltage exceeds 1.8V even during VID/DRFT transitions. The device will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the power or EN must be recycled to clear the latch.

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Outline Drawing - MLP-32



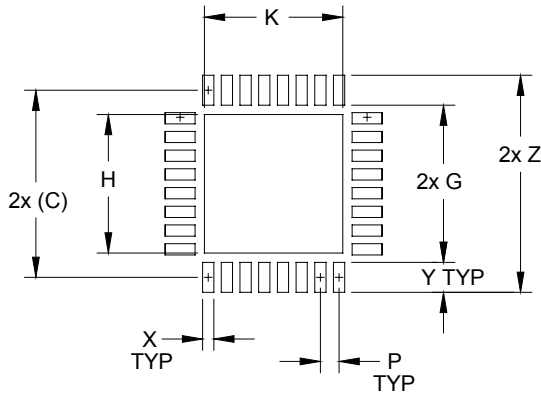
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

NOT RECOMMENDED FOR NEW DESIGN

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Land Pattern - MLP-32



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.197)	(5.00)
G	.165	4.20
H	.146	3.70
K	.146	3.70
P	.021	0.50
X	.012	0.30
Y	.031	0.80
Z	.228	5.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

NOT RECOMMENDED FOR NEW DESIGN

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