

### POWER MANAGEMENT

#### Description

The SC4520 is a current mode switching regulator with an integrated switch and an adjustable frequency with enable function. The integrated switch allows for cost-effective, low power solutions with a peak switch current of 3 amps. An adjustable high frequency of 100kHz to 600kHz provides for fast dynamic response and instantaneous duty cycle adjustment as the input varies, making the device ideal for CPE applications where the input is a wall plug power. Low shutdown current also makes this device an excellent choice for portable applications where conserving battery life is of prime concern.

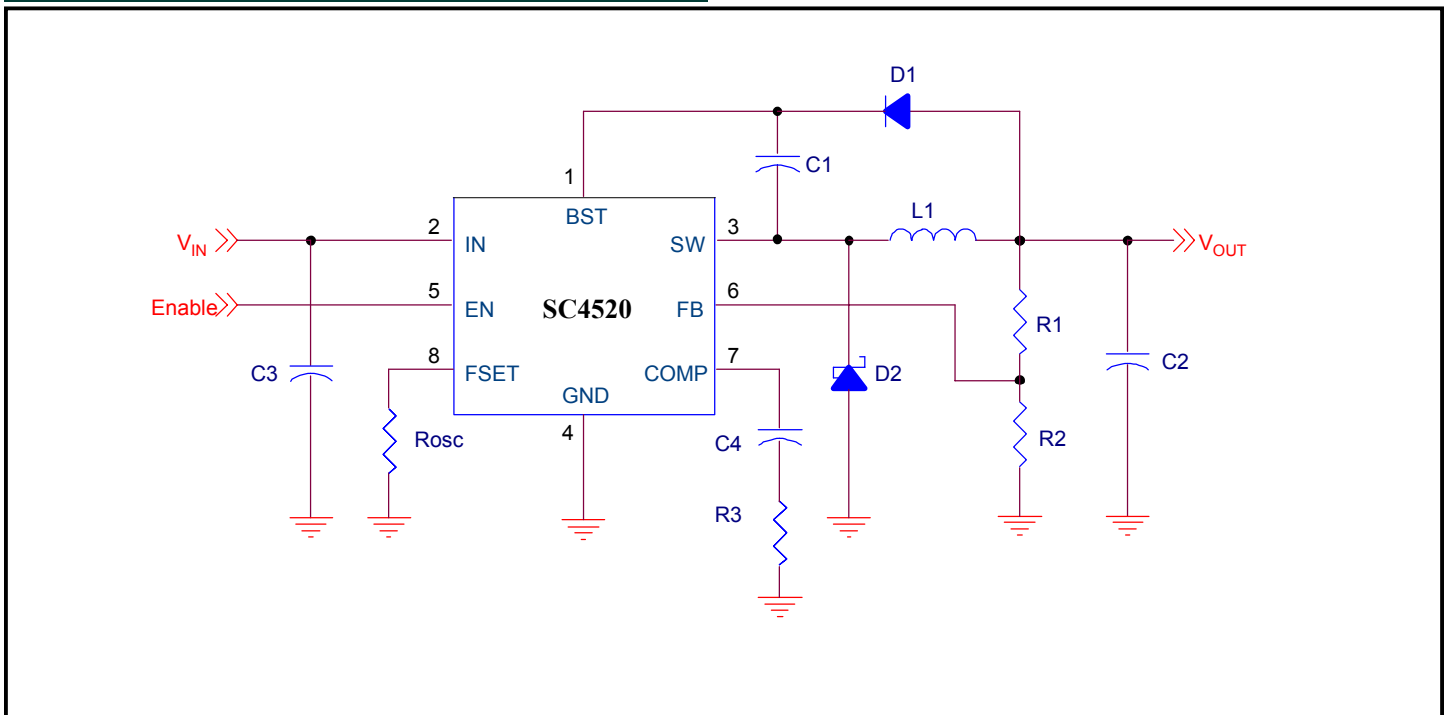
#### Features

- ◆ Wide operating voltage range: 4.4V to 24V
- ◆ Integrated 3 Amp switch
- ◆ 100kHz to 600kHz adjustable frequency operation
- ◆ Current mode control
- ◆ Precision enable threshold
- ◆ SO-8 EDP package. Lead-free product, fully WEEE and RoHS compliant

#### Applications

- ◆ XDSL modems
- ◆ CPE equipment
- ◆ DC-DC point of load applications
- ◆ Portable equipment
- ◆ Digital consumer electronics

#### Typical Application Circuit



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Limits	Units
Input Supply Voltage	$V_{IN}$	-0.3 to +28	V
Boost Pin Above $V_{SW}$	$(V_{BST} - V_{SW})$	16	V
Boost Pin Voltage	$V_{BST}$	-0.3 to +32	V
EN Pin Voltage	$V_{EN}$	-0.3 to +24	V
FB Pin Voltage	$V_{FB}$	-0.3 to +6	V
FB Pin Current	$I_{FB}$	1	mA
FSET Pin Voltage	$V_{FSET}$	+3	V
Thermal Impedance Junction to Ambient <sup>(1)</sup>	$\theta_{JA}$	36.5	°C/W
Maximum Junction Temperature	$T_J$	150	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	$T_{LEAD}$	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Note: (1) Minimum pad size.

**Electrical Characteristics**

Unless specified:  $V_{IN} = 12V$ ,  $V_{COMP} = 0.8V$ ,  $V_{BST} = V_{IN} + 5V$ , EN = tied to  $V_{IN}$ , SW = open.  
 $T_A = T_J = -40^{\circ}C$  to  $125^{\circ}C$ .

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Input Voltage	$V_{IN}$				24 <sup>(1)</sup>	V
Maximum Switch Current Limit	$I_{SW}$		3.0			A
Oscillator Frequency	$f_{OSC}$	$R_{OSC} = 82.5k \Omega$	250	300	350	kHz
Oscillator Frequency Range	$f_{OSC}$		100		600	kHz
Switch On Voltage Drop	$V_{D(SW)}$	$I_{SW} = 3A$		220		mV
$V_{IN}$ Undervoltage Lockout	$V_{UVLO}$			3.9	4.4	V
$V_{IN}$ UVLO Hysteresis	$V_{HYST}$			60		mV
$V_{IN}$ Supply Current	$I_Q$	$V_{FB} = 1V$		3	5.5	mA
Standby Current	$I_{Q(OFF)}$	$V_{EN} = 0V$		250		$\mu A$

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**Electrical Characteristics (Cont.)**

Unless specified:  $V_{IN} = 12V$ ,  $V_{COMP} = 0.8V$ ,  $V_{BST} = V_{IN} + 5V$ , EN = tied to  $V_{IN}$ , SW = open.  
 $T_A = T_J = -40^{\circ}C$  to  $125^{\circ}C$ .

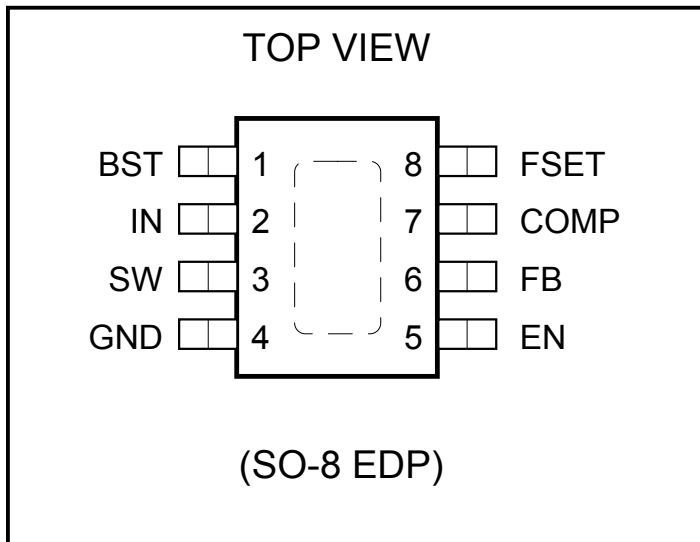
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Input Current	$I_{FB}$			-0.25	-1	$\mu A$
Feedback Voltage			0.784	0.8	0.816	V
Feedback Voltage Line Regulation		$4.4V < V_{IN} < 24V^{(1)}$		+3		mV/V
FB to $V_{COMP}$ Voltage Gain <sup>(2)</sup>		$0.9V \leq V_{COMP} \leq 2.0V$	150	350		V/V
FB to $V_{COMP}$ Transconductance <sup>(2)</sup>		$\Delta I_{COMP} = \pm 10\mu A$	500	850	1300	$\mu Mho$
$V_{COMP}$ Pin Source Current		$V_{FB} = 0.6V$		70	110	$\mu A$
$V_{COMP}$ Pin Sink Current		$V_{FB} = 1.0V$		-70	-110	$\mu A$
$V_{COMP}$ Pin to Switch Current Transconductance		$V_{COMP} = 1.25V$		4.3		A/V
$V_{COMP}$ Pin Maximum Switching Threshold		Duty cycle = 0%		0.6		V
$V_{COMP}$ OCP Threshold		$V_{COMP}$ rising		2		V
$V_{COMP}$ Hiccup Retry Threshold		$V_{COMP}$ falling		0.25		V
Maximum Switch Duty Cycle		$V_{COMP} = 1.2V$ , $I_{SW} = 400mA$ , $R_{OSC} = 0$	85			%
Minimum Boost Voltage Above Switch <sup>(2)</sup>				2.7		V
Boost Current		$I_{SW} = 1A$		10	15	mA
		$I_{SW} = 3A$		30	45	
Enable Input Threshold Voltage	$V_{ETH}$		1.1	1.3	1.5	V
Enable Output Bias Current	$I_{EOL}$	EN = 50mV below threshold		8		$\mu A$
	$I_{EOH}$	EN = 50mV below threshold		10		$\mu A$

**Notes:**

- (1) The required minimum input voltage for a regulated output depends on the output voltage and load condition.  
(2) Guaranteed by design.

**POWER MANAGEMENT**

**Pin Configurations**



**Ordering Information**

Part Number <sup>(1)(2)</sup>	Package
SC4520SETRT	SO-8 EDP
SC4520EVB	EVALUATION BOARD

**Notes:**

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

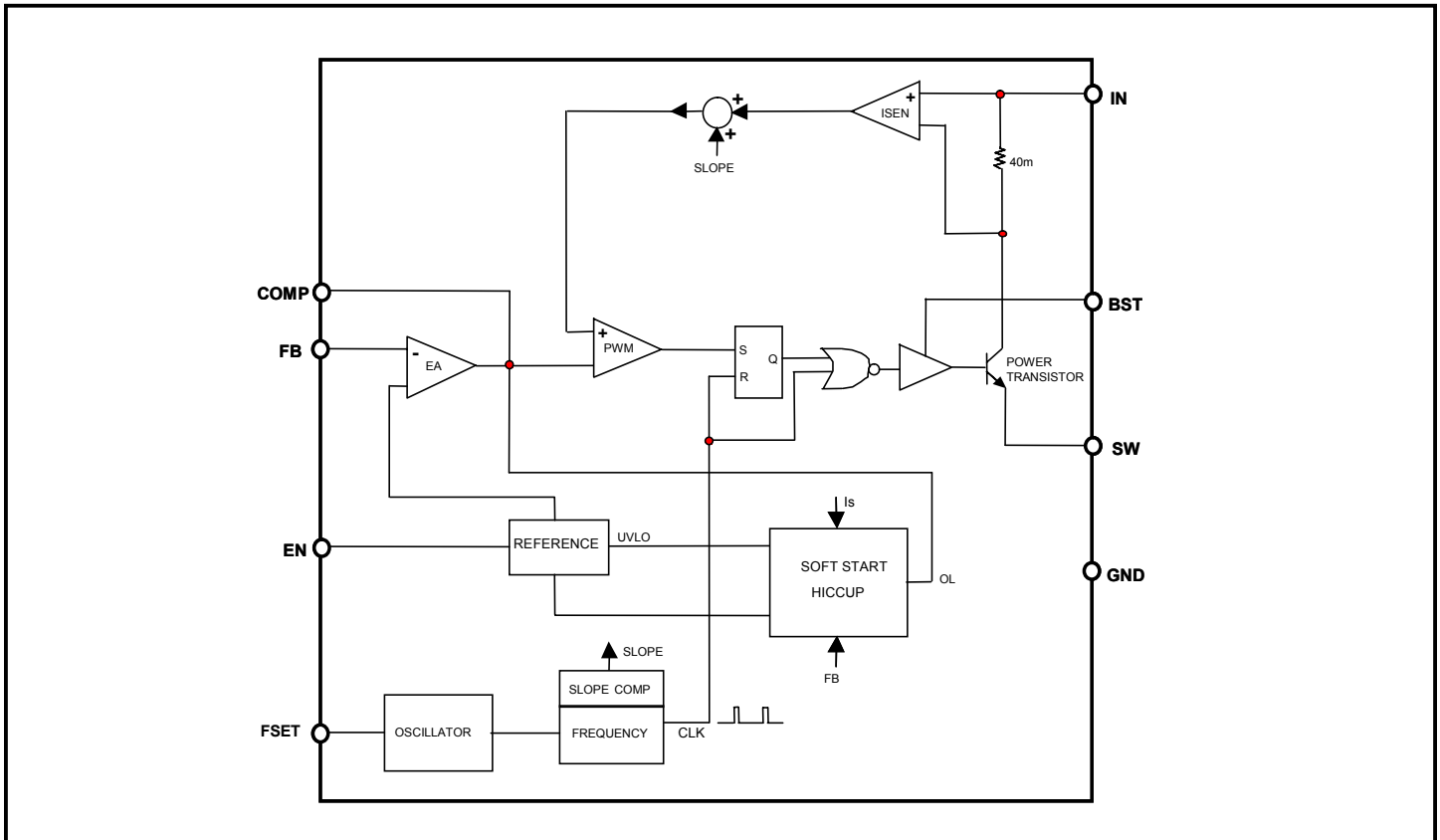
(2) Lead-free product. This product is WEEE and RoHS compliant.

**Pin Descriptions**

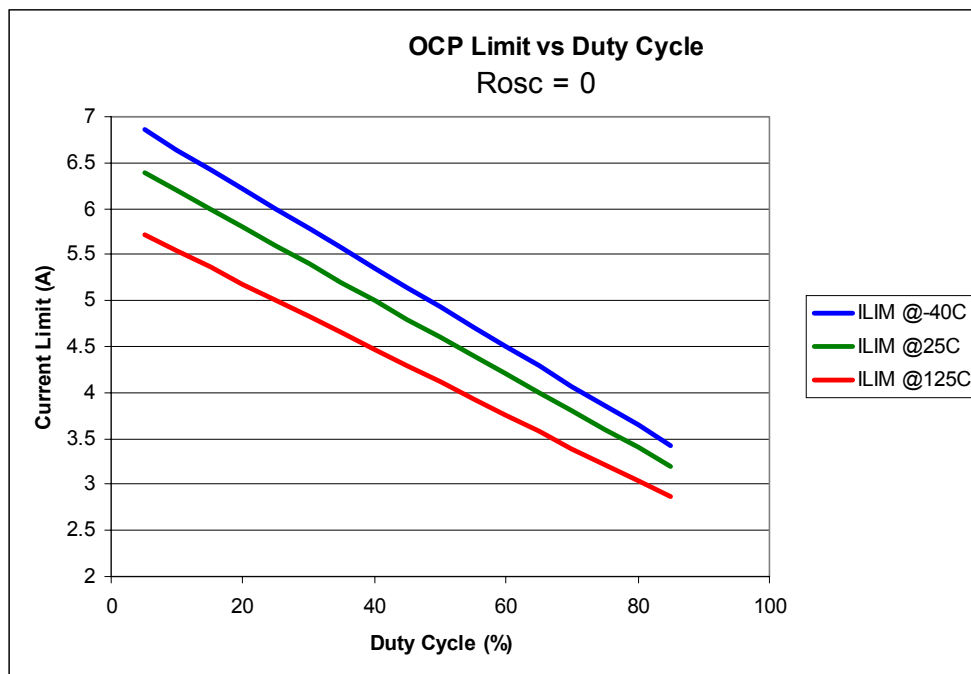
Pin #	Pin Name	Pin Function
1	BST	This pin provides power to the internal NPN switch. The minimum turn on voltage for this switch is 2.7V.
2	IN	Pin IN delivers all power required by control and power circuitry. This pin sees high di/dt during switching. A decoupling capacitor should be attached to this pin as close as possible.
3	SW	Pin SW is the emitter of the internal switch. The external freewheeling diode should be connected as close as possible to this pin.
4	GND	All voltages are measured with respect to this pin. The decoupling capacitor and the freewheeling diode should be connected to GND as short as possible.
5	EN	This is the chip enable input. The regulator is switched on if EN is high, and it is off if EN is low. The regulator is in standby mode when EN is low, and the input supply current is reduced to a few microamperes.
6	FB	Feedback input for adjustable output controllers.
7	COMP	This is the output of the internal error amplifier and input of the peak current comparator. A compensation network is connected to this pin to achieve the specified performance.
8	FSET	Frequency setting pin. An external resistor connected from this pin to GND, sets the oscillator frequency.
-	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

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**Block Diagram**



**Typical Characteristic - OCP Limit**



**POWER MANAGEMENT**

**Application Information**

The SC4520 is a current mode buck converter regulator. SC4520 has an internal fixed-frequency clock. The SC4520 uses two feedback loops that control the duty cycle of the internal power switch. The error amplifier functions like that of the voltage mode converter. The output of the error amplifier works as a switch current reference. This technique effectively removes one of the double poles in the voltage mode system. With this, it is much simpler to compensate a current mode converter to have better performance. The current sense amplifier in the SC4520 monitors the switch current during each cycle. Overcurrent protection (OCP) is triggered when the current limit exceeds the upper limit of 3A, detected by a voltage on COMP greater than about 2V. When an OCP fault is detected, the switch is turned off and the external COMP capacitor is discharged at the rate of  $dv/dt = 3\mu A/C_{comp}$ . Once the COMP voltage has fallen below 250mV, the part enters a normal startup cycle.  $C_{comp}$  is the total capacitance value attached to COMP. In the case of sustained overcurrent or dead-short, the part will continually cycle through the retry sequence as described above, at a rate dependent on the value of Ccomp. During start up, the voltage on COMP rises roughly at the rate of  $dv/dt = 120\mu A/C_{comp}$ . Therefore, the retry time for a sustained overcurrent can be approximately calculated as:

$$T_{retry} = C_{comp} \cdot \frac{2V}{120\mu A} + C_{comp} \cdot \frac{2V}{3\mu A}$$

Figure 1 shows the voltage on COMP during a sustained overcurrent condition.

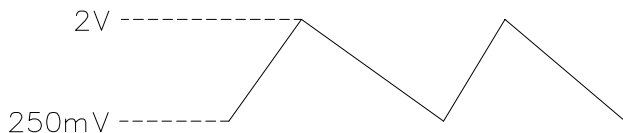


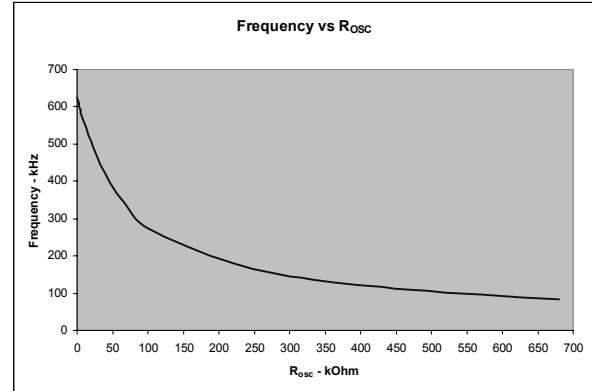
Figure 1. Voltage on COMP for Startup and OCP

**Enable**

Pulling and holding the EN pin below 0.4V activates the shut down mode of the SC4520 which reduces the input supply current to less than 150µA. During the shut down mode, the switch is turned off. The SC4520 is turned on if the EN pin is pulled high.

**Oscillator**

The external resistor connected to the FSET pin sets the PWM frequency from 100kHz to 600kHz.



**UVLO**

When the EN pin is pulled and held above 1.8V, the voltage on Pin IN determines the operation of the SC4520. As  $V_{IN}$  increases during power up, the internal circuit senses  $V_{IN}$  and keeps the power transistor off until  $V_{IN}$  reaches 4.4V.

**Load Current**

The peak current  $I_{PEAK}$  in the switch is internally limited. For a specific application, the allowed load current  $I_{OMAX}$  will change if the input voltage drifts away from the original design as given for continuous current mode:

$$I_{OMAX} = 3 - \frac{V_o \cdot (1-D)}{2 \cdot L \cdot f_s}$$

Where:

- $f_s$  = switching frequency,
- $V_o$  = output voltage and
- $D$  = duty ratio,  $V_o / V_{IN}$
- $V_{IN}$  = input voltage.

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**Application Information (Cont.)**

Figure 2 shows the theoretical maximum load current for the specific cases. In a real application, however, the allowed maximum load current also depends on the layout and the air cooling condition. Therefore, the maximum load current may need to be degraded according to the thermal situation of the application.

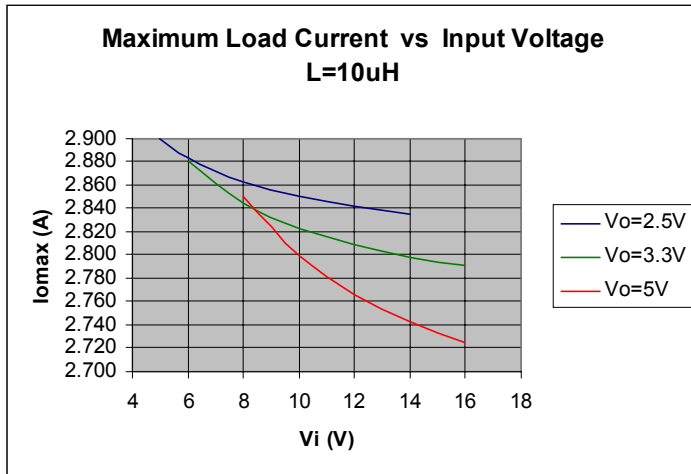


Figure 2. Theoretical maximum load current curves

**Inductor Selection**

The factors for selecting the inductor include its cost, efficiency, size and EMI. For a typical SC4520 application, the inductor selection is mainly based on its value, saturation current and DC resistance. Increasing the inductor value will decrease the ripple level of the output voltage while the output transient response will be degraded. Low value inductors offer small size and fast transient responses while they allow large ripple currents, poor efficiencies and require more output capacitance for low output ripple. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss. A good trade-off among its size, loss and cost is to set the inductor ripple current to be within 15% to 30% of the maximum output current.

The inductor value can be determined according to its operating point under its continuous mode and the switching frequency as follows:

$$L = \frac{V_O \cdot (V_I - V_O)}{V_I \cdot f_s \cdot \delta \cdot I_{OMAX}}$$

Where:

fs = switching frequency,

δ = ratio of the peak to peak inductor current to the output load current and

Vo = output voltage.

The peak to peak inductor current is:

$$I_{p-p} = \delta \cdot I_{OMAX}$$

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency specifications. The core must be able to handle the peak inductor current  $I_{PEAK}$  without saturation and produce low core loss during the high frequency operation.

$$I_{PEAK} = I_{OMAX} + \frac{I_{p-p}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core must be able to handle the peak inductor current  $I_{PEAK}$  without saturation and produce low core loss during the high frequency operation. The core loss can be found in the manufacturer's datasheet. The inductor's copper loss can be estimated as follows:

$$P_{COPPER} = I_{LRMS}^2 \cdot R_{WINDING}$$

Where:

$I_{LRMS}$  is the RMS current in the inductor. This current can be calculated as follows:

$$I_{LRMS} = I_{OMAX} \cdot \sqrt{1 + \frac{1}{12} \cdot \delta^2}$$

**Output Capacitor Selection**

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the output voltage deviation during load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the SC4520 regulates the inductor current to a new value during a

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**Application Information (Cont.)**

load transient, the output capacitor delivers all the additional current needed by the load. The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple. Surface mount ceramic capacitors are recommended.

**Input Capacitor Selection**

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current drawn by the converter. For the continuous conduction mode, the RMS value of the input capacitor current  $I_{CIN(RMS)}$  can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \cdot \sqrt{\frac{V_O \cdot (V_I - V_O)}{V^2_I}}$$

This current gives the capacitor's power loss through its  $R_{CIN(ESR)}$  as follows:

$$P_{CIN} = I_{CIN(RMS)}^2 \cdot R_{CIN(ESR)}$$

The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \cdot \frac{D \cdot (1 - D)}{f_s \cdot (\Delta V_I - I_{OMAX} \cdot R_{CIN(ESR)})}$$

Where:

$\Delta V_I$  = the given input voltage ripple.

Because the input capacitor is exposed to the large surge current, attention is needed for the input capacitor. If tantalum capacitors are used at the input side of the converter, one needs to ensure that the RMS and surge ratings are not exceeded. For generic tantalum capacitors, it is suggested to derate their voltage ratings at a ratio of about two to protect these input capacitors.

**Boost Capacitor and its Supply Source Selection**

The boost capacitor selection is based on its discharge ripple voltage, worst case conduction time and boost current. The worst case conduction time  $T_w$  can be estimated as follows:

$$T_w = \frac{1}{f_s} \cdot D_{max}$$

Where:

$f_s$  = the switching frequency and

$D_{max}$  = maximum duty ratio, 0.85 for the SC4520.

The required minimum capacitance for the boost capacitor will be:

$$C_{boost} = \frac{I_B}{V_D} \cdot T_w$$

Where:

$I_B$  = the boost current and

$V_D$  = discharge ripple voltage.

With  $f_s = 600kHz$ ,  $V_D = 0.5V$  and  $I_B = 0.045A$ , the required minimum capacitance for the boost capacitor is:

$$C_{boost} = \frac{I_B}{V_D} \cdot \frac{1}{f_s} \cdot D_{max} = \frac{0.045}{0.5} \cdot \frac{1}{600k} \cdot 0.85 = 128nF$$

The internal driver of the switch requires a minimum 2.7V to fully turn on that switch to reduce its conduction loss. If the output voltage is less than 2.7V, the boost capacitor can be connected to either the input side or an independent supply with a decoupling capacitor. But the Pin BST should not see a voltage higher than its maximum rating.

**Freewheeling Diode Selection**

This diode conducts during the switch's off-time. The diode should have enough current capability for full load and short circuit conditions without any thermal concerns. Its maximum repetitive reverse block voltage has to be higher than the input voltage of the SC4520. A low forward conduction drop is also required to increase the overall efficiency. The freewheeling diode should be turned on and off fast with minimum reverse recovery because the SC4520 is designed for high frequency applications. SS23 Schottky rectifier is recommended for certain applications. The average current of the diode,  $I_{D-AVG}$  can be calculated by:

$$I_{D-AVG} = I_{omax} \cdot (1 - D)$$

**POWER MANAGEMENT**

**Application Information (Cont.)**

**Thermal Considerations**

There are three major power dissipation sources for the SC4520. The internal switch conduction loss, its switching loss due to the high frequency switching actions and the base drive boost circuit loss. These losses can be estimated as:

$$P_{total} = I_o^2 \cdot R_{on} \cdot D + 10.8 \cdot 10^{-3} \cdot I_o \cdot V_I + \frac{10}{1000} \cdot I_o \cdot D \cdot (V_{boost})$$

Where:

$I_o$  = load current;

$R_{on}$  = on-equivalent resistance of the switch;

$V_{BOOST}$  = input voltage or output based on the boost circuit connection.

The junction temperature of the SC4520 can be further determined by:

$$T_J = T_A + \theta_{JA} \cdot P_{total}$$

$\theta_{JA}$  is the thermal resistance from junction to ambient. Its value is a function of the IC package, the application layout and the air cooling system.

The freewheeling diode also contributes a significant portion of the total converter loss. This loss should be minimized to increase the converter efficiency by using Schottky diodes with low forward drop ( $V_F$ ).

$$P_{diode} = V_F \cdot I_o \cdot (1-D)$$

**Loop Compensation Design**

The SC4520 has an internal error amplifier and requires a compensation network to connect between the COMP pin and GND pin as shown in Figure 3. The compensation network includes C4, C5 and R3. R1 and R2 are used to program the output voltage according to:

$$V_O = 1.2 \cdot \left(1 + \frac{R_1}{R_2}\right)$$

Assuming the power stage ESR (equivalent series resistance) zero is an order of magnitude higher than the closed loop bandwidth, which is typically one tenth of the switching frequency, the power stage control to output transfer function with the current loop closed (Ridley model) for the SC4520 will be as follows:

$$G_{VD}(s) = \frac{4.3 \cdot R_L}{1 + \frac{s}{\frac{1}{R_L \cdot C}}}$$

Where:

$R_L$  – Load and

$C$  – Output capacitor.

The goal of the compensation design is to shape the loop to have a high DC gain, high bandwidth, enough phase margin, and high attenuation for high frequency noises. Figure 3 gives a typical compensation network which offers 2 poles and 1 zero to the power stage:

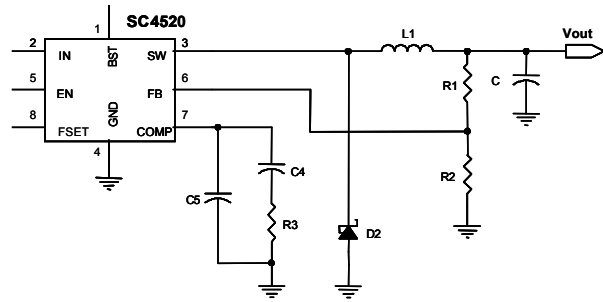


Figure 3. Compensation network provides 2 poles and 1 zero.

The compensation network gives the following characteristics:

$$G_{COMP}(s) = \omega_1 \cdot \frac{1 + \frac{s}{\omega_Z}}{s \cdot \left(1 + \frac{s}{\omega_{P2}}\right)} \cdot g_m \cdot \frac{R_2}{R_1 + R_2}$$

Where:

$$\omega_1 = \frac{1}{C_4 + C_5}$$

$$\omega_Z = \frac{1}{R_3 \cdot C_4}$$

$$\omega_{P2} = \frac{C_4 + C_5}{R_3 \cdot C_4 \cdot C_5}$$

The loop gain will be given by:

$$T(s) = G_{COMP}(s) \cdot G_{VD}(s) = 3.655 \cdot 10^{-3} \cdot \frac{R_L}{C_4} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{1}{s} \cdot \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_{P1}}\right) \cdot \left(1 + \frac{s}{\omega_{P2}}\right)}$$

Where:

$$\omega_{P1} = \frac{1}{R_L \cdot C}$$

**POWER MANAGEMENT**
**Application Information (Cont.)**

One integrator is added at origin to increase the DC gain.  $\omega_z$  is used to cancel the power stage pole  $\omega_{p1}$  so that the loop gain has  $-20\text{dB/dec}$  rate when it reaches  $0\text{dB}$  line.  $\omega_{p2}$  is placed at half switching frequency to reject high frequency switching noises. Figure 4 gives the asymptotic diagrams of the power stage with current loop closed and its loop gain.

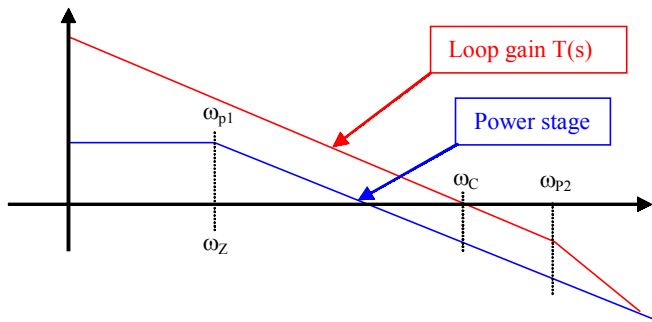


Figure 4. Asymptotic diagrams of power stage with current loop closed and its loop gain.

The design guidelines for the SC4520 applications are as following:

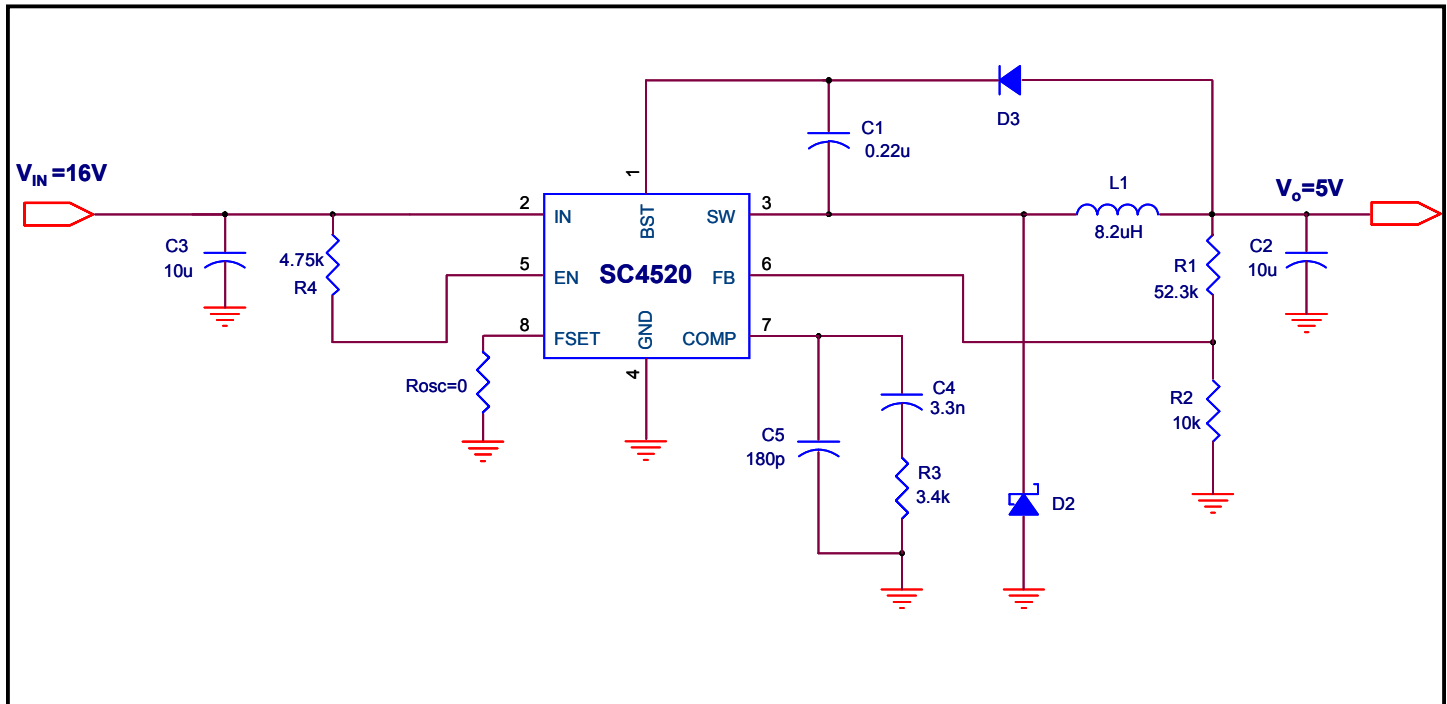
1. Set the loop gain crossover corner frequency  $\omega_c$  for given switching corner frequency  $\omega_c = 2\pi f_c$
2. Place an integrator at the origin to increase DC and low frequency gains.
3. Select  $\omega_z$  such that it is placed at  $\omega_{p1}$  to obtain a  $-20\text{dB/dec}$  rate to go across the  $0\text{dB}$  line.
4. Place a high frequency compensator pole  $\omega_{p2}$  ( $\omega_{p2} = \pi f_s$ ) to get the maximum attenuation of the switching ripple and high frequency noise with the adequate phase lag at  $\omega_c$ .

**Layout Guidelines:**

In order to achieve optimal electrical and thermal performance for high frequency converters, special attention must be paid to the PCB layouts. The goal of layout optimization is to identify the high  $di/dt$  loops and minimize them. The following guidelines should be used to ensure proper operation of the converters.

1. A ground plane is suggested to minimize switching noises and trace losses and maximize heat transferring.

2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all power connections on one side of the PCB with wide copper filled areas if possible.
3. The  $V_{IN}$  bypass capacitor should be placed next to the  $V_{IN}$  and GND pins.
4. The trace connecting the feedback resistors to the output should be short, direct and far away from any noise sources such as switching node and switching components.
5. Minimize the loop including input capacitor, the SC4520 and freewheeling diode  $D_2$ . This loop passes high  $di/dt$  current. Make sure the trace width is wide enough to reduce copper losses in this loop.
6. Maximize the trace width of the loop connecting the inductor, freewheeling diode  $D_2$  and the output capacitor.
7. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC4520 by using a separate ground trace.
8. Connect Pin 4 to a large copper area to remove the IC heat and increase the power capability of the SC4520. A few feedthrough holes are required to connect this large copper area to a ground plane to further improve the thermal environment of the SC4520. The traces attached to other pins should be as wide as possible for the same purpose.

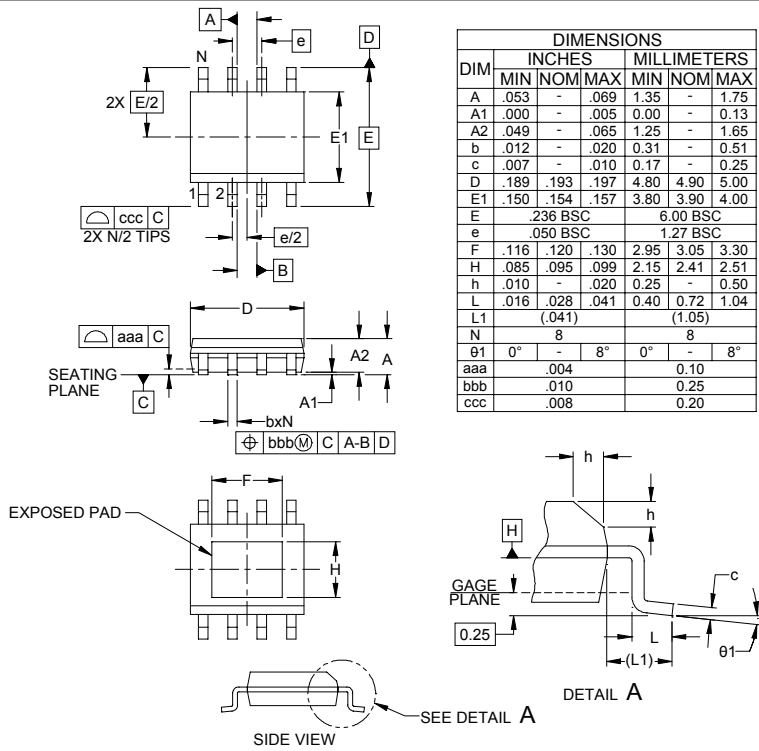
**POWER MANAGEMENT**
**Application Information (Cont.)**
**Design Example: 16V to 5V at 2A**

**Bill of Materials**

Item	Qty	Reference	Value	Part No./Manufacturer
1	1	C1	0.22uF, 25V, 0805, X7R	Vishay
2	2	C2, C3	10u, 1210, X5R, 25V	Panasonic
3	1	C4	3.3n, 0805, X7R, 25V	Vishay
4	1	C5	180pF	
5	1	D1	1N4148WS, SOD-323	
6	1	D2	SS33	Fairchild P/N: SS33
7	1	L1	8.2uH	COOPER P/N:DR125-8R2
8	1	R1	52.3K	
9	1	R2	10k	
10	1	R3	3.4k	
11	1	R4	4.75k	
12	1	Rosc	0	
13	1	U1	SC4520	Semtech

Unless specified, all resistors have 1% precision with 0603 package.  
Resistors are +/-1% and all capacitors are +/-20%

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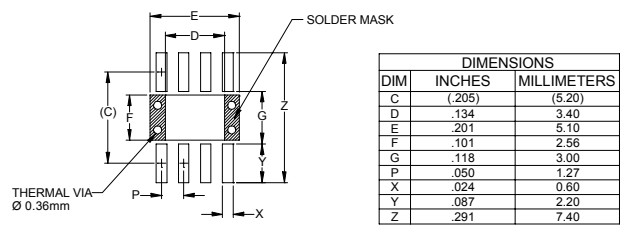
**Outline Drawing - SOIC-8L EDP**



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.116	.120	.130	2.95	3.05	3.30
H	.085	.095	.099	2.15	2.41	2.51
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MS-012, VARIATION BA.

**Land Pattern - SOIC-8L EDP**



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A, RLP NO. 300A.
  3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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