

POWER MANAGEMENT
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
BST, GDH to PGND		-0.3 to 32 (steady state)	V
		-0.3 to 40 (for < 10ns @ freq. < 500kHz)	
PVCC, AVCC, VIN, VPIN, GDL to PGND		-0.3 to 16	V
PGND to AGND		±0.3	V
CS± to AGND		-0.3 to AVCC	V
COMP, IN-, REFIN, REFOUT, ROSC, SS/EN to AGND		-0.3 to 6	V
REFIN and REFOUT to AGND		0 to 3.0	V
GDH Source or Sink Current		± 0.75	A
GDL Source or Sink Current		± 1	A
Storage Temperature Range		-60 to +150	°C
Junction Temperature		-40 to +125	°C
Lead Temperature (Soldering) 10 Sec.		260	°C
ESD Rating (Human Body Model)		2	kV

Electrical Characteristics

Unless specified: T_A = T_J = -40°C to +85°C, AVCC/PVCC = 12V, Fosc = 300 kHz, SS/EN = 5V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Operating Current		No load on GDL and GDH		8	12	mA
Analog Supply Input	AVCC	VIN > 2.5V	4.75		16	V
Drive Supply Input	PVCC	VIN > 2.5V	4.75		16	V
Convertor Power Input	VIN		2.5		16	V
Undervoltage Lockout						
Start Threshold	AVCC _{MIN}		4.2	4.5	4.7	V
UVLO Hysteresis	AVCC _{HYST}			0.2		V
Soft Start and Shutdown						
Charge Current	I _{SSCHG}			2		µA
Discharge Current	I _{SSDIS}			1		µA
Output Enable Threshold	V _{ENTH}		2.0			V
Shutdown Threshold	V _{SSTH}				0.6	V

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Electrical Characteristics (Cont.)

 Unless specified: $T_A = T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $AVCC/PVCC = 12\text{V}$, $F_{osc} = 300\text{ kHz}$, $SS/EN = 5\text{V}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier						
Input Bias Current				0.4	0.7	μA
Input Offset Voltage					2.5	mV
Transconductance Gain	G_M	Output Source Mode Output Sink Mode		275 375		$\mu\Omega^{-1}$
Unity Gain Bandwidth ⁽¹⁾				3		MHz
Output Sink/Source Current		$V_{COMP} = 2.5\text{V}$		15		μA
Buffered Reference						
Internal reference	V_{REF}	-40C to +85C	0.49	0.5	0.51	V
Line regulation		$5\text{V} < AVCC < 15\text{V}$		0.02		%/V
External reference input range	V_{REFIN}		0.3		3.0	V
Tracking accuracy	V_{REFOUT}	With respect to V_{REFIN} (Greater of the two)			± 0.5 ± 10.0	% mV
Reference output current	I_{REFOUT}			5		mA
Oscillator and Synchronisation						
Frequency range	F_{osc}		0.1		1	MHz
Frequency setting	F_{osc}	ROSC = 221K	270	300	330	KHz
Sync input High voltage			1.5			V
Sync input Low voltage					0.5	V
Duty Cycle						
Maximum Duty Cycle		$F_{osc} = 1\text{ MHz}$		70		%
		$F_{osc} = 300\text{ kHz}$		90		%
Minimum Duty Cycle		$F_{osc} = 100\text{ kHz}$		5		%
Minimum pulse width		$F_{osc} = 0.1\text{ to }1\text{ MHz}$		250		nS
Current Limit						
Current limit sense threshold	V_{CSLIM}	Output source mode	60	75	90	mV
		Output sink mode	-85	-110	-130	mV
Delay to Output ⁽¹⁾	t_{CSDLY}	10 mV Overdrive		50		nS

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Electrical Characteristics (Cont.)

 Unless specified: $T_A = T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $AVCC/PVCC = 12\text{V}$, $F_{\text{osc}} = 300\text{ kHz}$, $SS/EN = 5\text{V}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Output						
Overvoltage sense threshold	V_{OVTH}	REFIN = 2.5V		2.8		V
Undervoltage sense threshold	V_{UVTH}	REFIN = 2.5V		2.2		V
Power Good voltage	V_{PG}	$I_{\text{PG}} = 5\text{ mA}$ $I_{\text{PG}} = 2.5\text{ mA}$ Output under fault		1.5	0.4	V V
Output Drive						
High Side Gate Drive	I_{GDH}	Source or sink		1		A
Low Side Gate Drive	I_{GDL}	Source or sink		1		A
Dead Time Between Drives			60	90	120	nS
Rise Time		$C_{\text{OUT}} = 1000\text{ pF}$		20		nS
Fall Time		$C_{\text{OUT}} = 1000\text{ pF}$		20		nS

Note:

(1) Guaranteed by design. Not tested in production.

Ordering Information

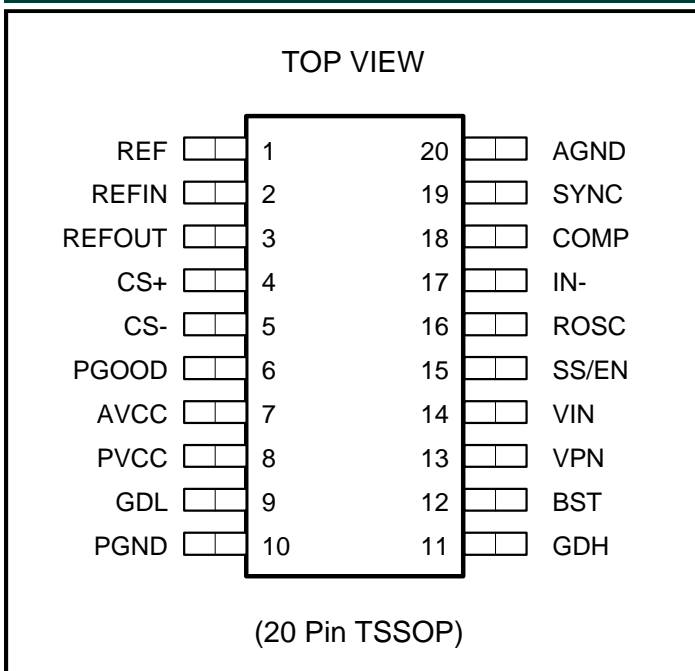
Part Number	Package ⁽¹⁾	Temp. Range (T_J)
SC4510ITSTR	TSSOP-20	-40°C to +85°C
SC4510ITSTR ⁽²⁾		

Notes:

(1) Only available in tape and reel packaging.

A reel contains 2500 devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Configuration


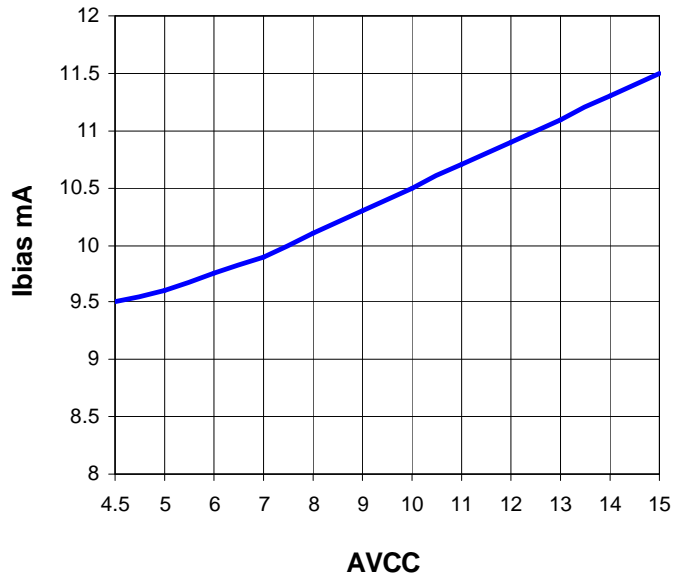
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Pin Descriptions

Pin #	Pin Name	Pin Function
1	REF	Internal 0.5V bandgap reference
2	REFIN	Non inverting input of the error amplifier. Can be connected to REF pin or an external voltage such as VDDQ/2. Maximum input range is 3V
3	REFOUT	Buffered reference output for external use. Tracks the REFIN voltage
4	CS+	Current sense input +ve
5	CS-	Current sense input -ve. Typically connected to the VOUT end of the output inductor.
6	PGOOD	Power Good output signal. Open collector output goes low under fault and sinks up to 5 mA. Monitors the output at thresholds of $\pm 12\%$ with respect to REFIN voltage.
7	AVCC	Supply voltage for internal analog circuits.
8	PVCC	Supply voltage for output drivers. Bypass with a large ceramic capacitor to PGND.
9	GDL	Gate drive output for the low side N-Channel MOSFET.
10	PGND	Power ground for returning the drive currents.
11	GDH	Gate drive output for the high side N-Channel MOSFET.
12	BST	Boost capacitor connection for the high side gate drive. Connect an external capacitor and a diode as shown in the Typical Application Circuit.
13	VPN	Virtual Phase Node. Auxiliary pin used for virtual current sense. Connect an RC between this pin and the VOUT end of the output inductor to sense the integrated current feedback signal.
14	VIN	Input supply for the virtual current sense circuit. This should be at the same potential as the drain of the high side power MOSFET.
15	SS/EN	Soft Start and Enable pin. Grounding the pin shuts down the controller. Connect a capacitor to soft start the output. The output will start switching when the SS pin voltage goes above 0.5V.
16	ROSC	Connect a resistor to AGND to program the oscillator frequency.
17	IN-	Inverting feedback input for the error amplifier. Follows the reference input provided at the REFIN pin. Maximum voltage range is 3V.
18	COMP	Error amplifier output for compensation.
19	SYNC	Pin for external synchronisation signal input
20	AGND	Analog signal ground. Return the ground connections of noise sensitive components such as ROSC, soft start capacitor, sync signal, feedback resistor chain and feedback compensation components separately to this pin.

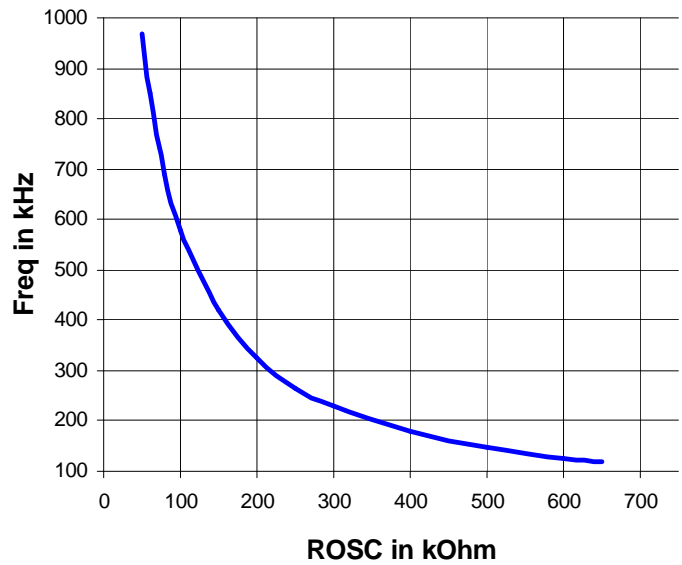
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Characteristic Curves

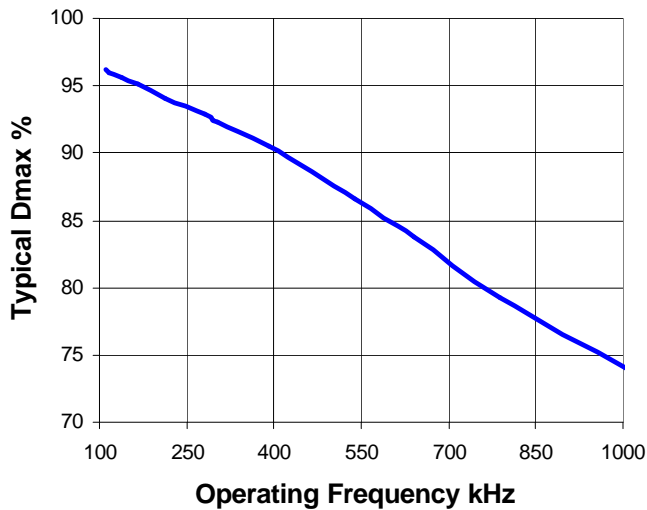
AVCC vs Bias Current



Operating Frequency vs ROSC



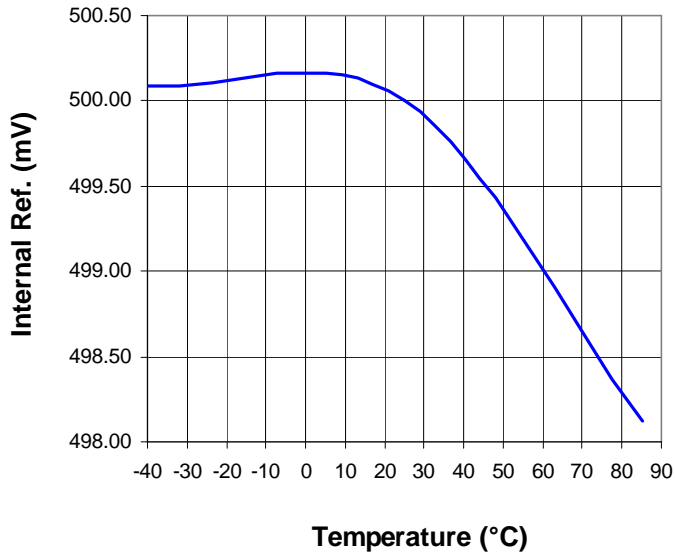
Typical Dmax vs Operating Frequency



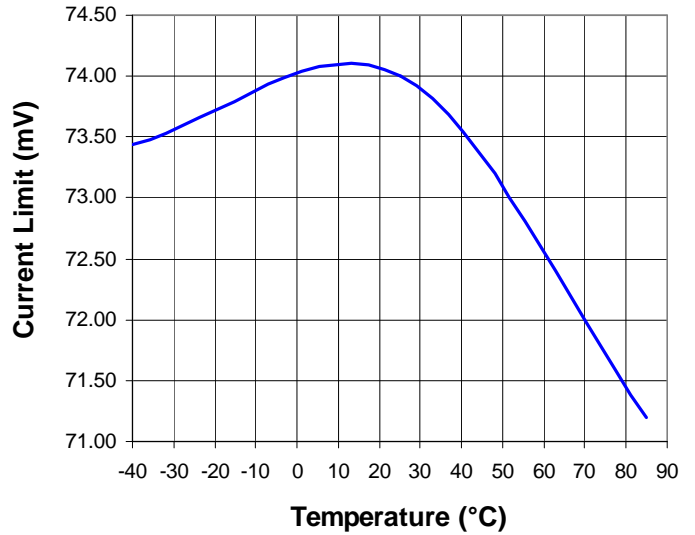
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Characteristic Curves

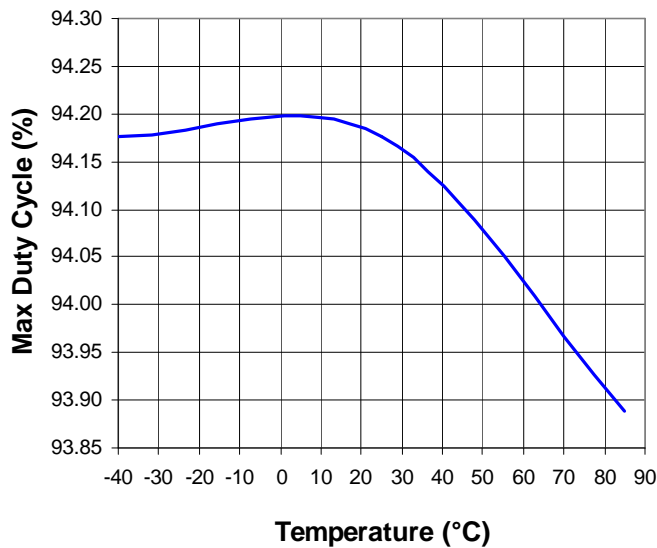
Internal Reference vs Temperature



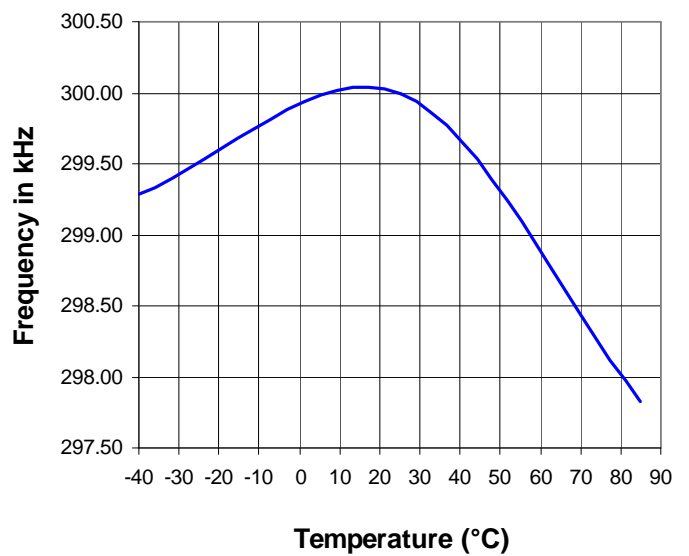
Current Limit vs Temperature



**Max Duty Cycle vs Temperature
@ RO SC = 220K**

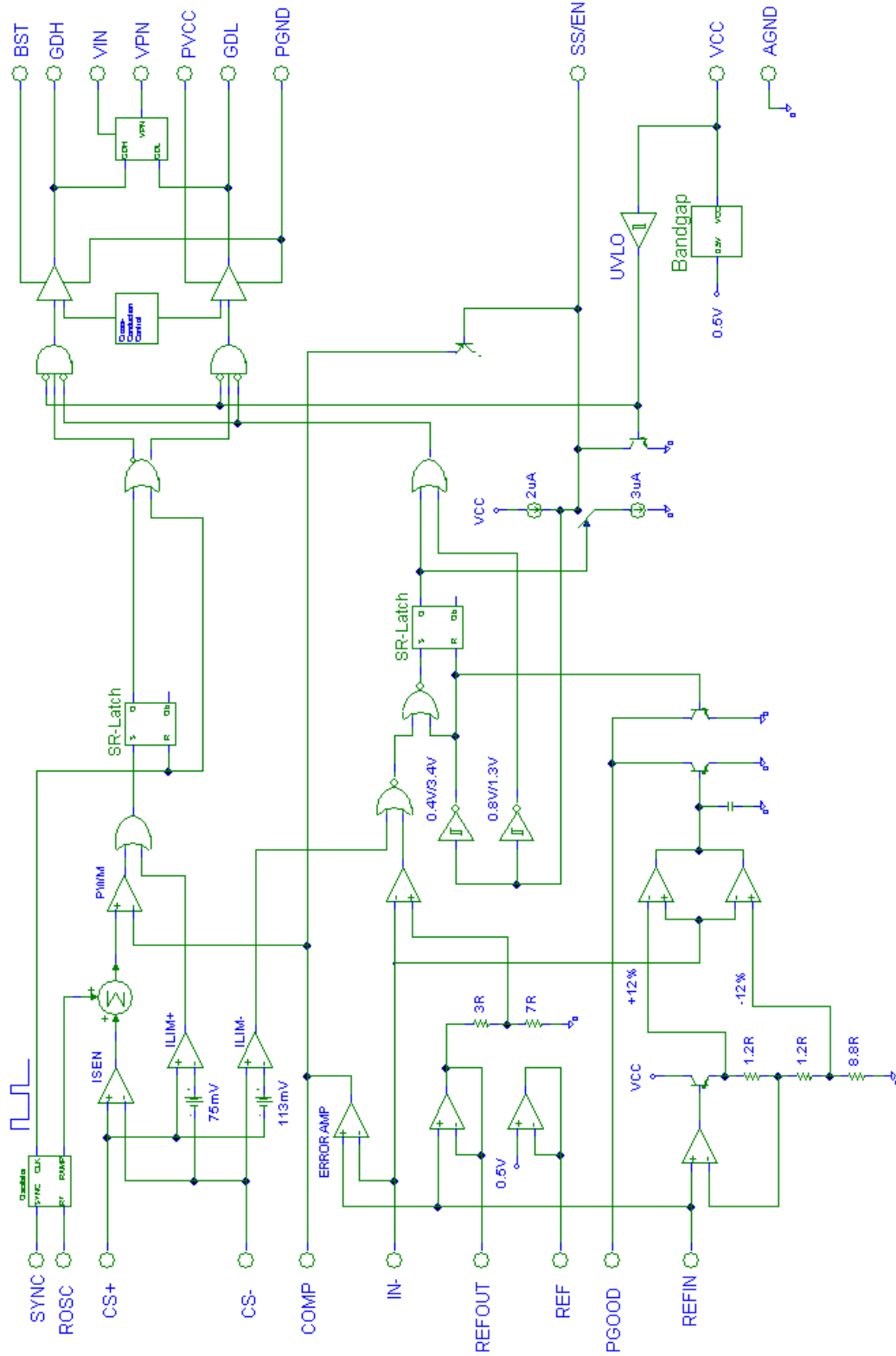


**Frequency vs Temperature
@ RO SC = 220K**



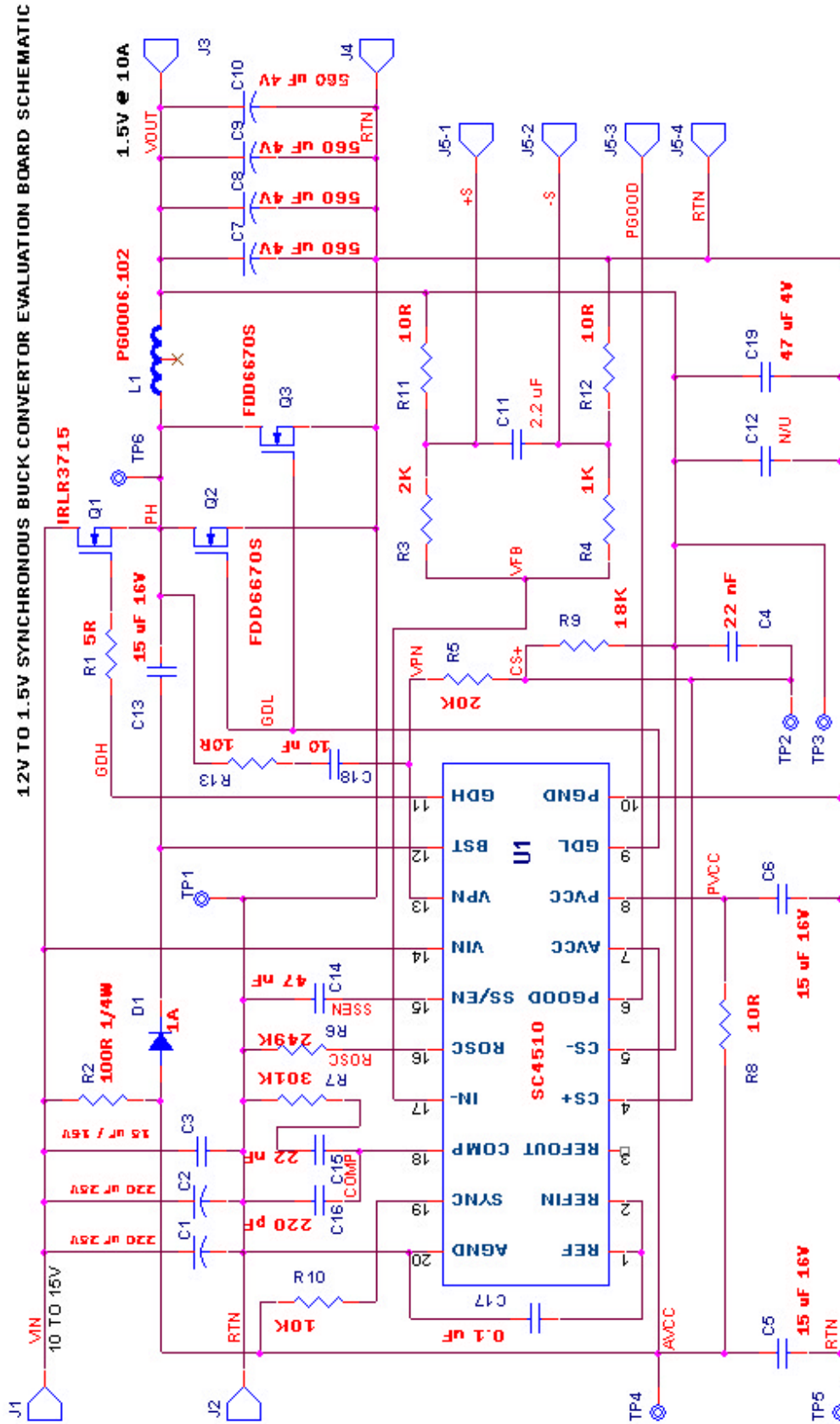
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Block Diagram



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Application Schematic



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Functional Description

INTRODUCTION

The SC4510 is designed to control and drive N-Channel MOSFET synchronous rectified buck convertors. It has additional features such as reference tracking, buffered REFOUT that make it particularly attractive for tracking output applications such as DDR memories. It can operate the convertor in both the source and sink modes. The switching frequency is programmable to optimize design. The current mode switching regulator section features Semtech's patented Combi Sense technique for lossless current sensing and provides a hiccup mode overcurrent protection.

POWERING THE CONTROLLER

Supplies VIN, PVCC and AVCC from the input source are used to power the SC4510. The AVCC and PVCC can be tied to VIN supply or can be from separate source to optimise efficiency. The AVCC supply provides the bias for the oscillator, PWM switcher, voltage feedback, current sense and the Power OK circuitry. PVCC is used to drive the low and high side MOSFET gates. Minimum operating limit for VIN is 2.5V typical. However, PVCC and AVCC have higher UVLO limits as explained below. Maximum range for all of the input and supply voltages is 16V.

STARTUP AND ENABLE

Startup is inhibited until AVCC input reaches its UVLO threshold. The UVLO limit is 4.5V typical. When AVCC is below the UVLO threshold, the soft start pin is pulled low and output drivers are turned off. The power up sequence is initiated by a 2 uA current source charging the soft start capacitor connected to the SS pin. When the SS pin reaches 0.5V, the convertor will start switching. The reference input of the error amplifier is ramped up with the soft-start signal. The soft start duration is controlled by the value of the SS cap. The soft start pin also functions as an enabler with TTL compatible input thresholds. If the SS/EN pin is pulled below 0.6V, the SC4510 is disabled and draws very low current.

REFERENCE INPUT AND BUFFERED OUTPUT

The SC4510 comes with a low level built in reference of 0.5V. The non inverting input of the error amplifier is brought out to provide additional flexibility and output tracking functions. In the basic operation, the REF and REFIN pins may be shorted together and the output voltage feedback is provided at IN- pin.

In tracking applications such as DDR memories an external reference may be brought in and applied at REFIN pin. The range of applicable external voltage is up to 3V. The UV and OV sensing thresholds for PGOOD output are centered $\pm 12\%$ around REFIN voltage.

The voltage at REFIN pin is buffered and put out as REFOUT. This output tracks REFIN accurately within ± 10 mV offset or 0.5% of REFIN, whichever is higher. It can also source up to 5 mA current. The REFOUT output is particularly useful in DDR memory termination applications.

OSCILLATOR

The switching frequency F_{osc} of the SC4510 is set by an external resistor using the following formula:

$$R_{osc} = 66,000 / F_{osc}$$

R_{osc} is in k Ω and F_{osc} is in kHz. The nominal range for the oscillator frequency is from 100 kHz to 1 MHz. The maximum duty cycle available at any given frequency is limited by minimum pulse width requirement which is typically 250 nS. This gives a typical Dmax of 70% at the highest frequency of 1 MHz or about 90% at 300 kHz.

The oscillator can be synchronised to an external clock that is nominally *faster* than the internal frequency set by R_{osc} . The synchronising signal should be TTL compatible, with transitions above 2.0V and below 0.6V. The external voltage level applied should be lower than AVCC of the device.

GATE DRIVERS

The low side gate driver is supplied from PVCC and provides a peak source/sink current of 1A. The high side gate drive is capable of sourcing and sinking peak currents of 0.75A. Protection logic provides a typical dead time of 90 nS to ensure both the upper and lower MOSFETs will not turn on simultaneously and cause a shoot through condition.

The high side Mosfet gate drive can be derived from the PVCC supply using the classical bootstrap technique as illustrated in the applications circuits. A bootstrap capacitor is connected from BST to the Phase node while PVCC is connected through a low V_F Schottky or an ultrafast diode to the BST. This will provide a gate to source voltage approximately equal to the $(VCC - V_{fwd})$.

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Functional Description

Alternately if an external 12V supply is available it can be directly connected between BST and GND. The actual gate to source voltage of the upper Mosfet will then be approximately be equal to $(12V - V_{IN})$. This technique is useful if the input voltage is 5V but a 12V supply is also available in the system.

POWER GOOD MONITOR

The PGOOD circuitry monitors the FB input of the convertor error amplifier. If the voltage on this input goes above +12% or below -12% of the REFIN voltage the PGOOD pin is pulled low. The PGOOD is an open drain output and can sink up to 5 mA. The PGOOD pin is held low during the startup sequence.

ERROR AMPLIFIER

The SC4510 is a current mode controller and operates by matching the peak of the sensed inductor current to the output of the voltage error amplifier. The error amplifier is transconductance type and should be compensated accordingly. It has a transconductance gain of $275 \mu\Omega^{-1}$ in the source mode. Current is sensed losslessly by taking the weighted average of both the MOSFET drops and adding it to the DC voltage drop across the inductor. More information on this patented Combi Sense technique is provided in the next section.

Current mode controllers are inherently unstable at duty ratios above 50% and need some form of slope compensation to operate correctly. This slope compensation is built into the architecture of SC4510 where a portion of the ramp is internally added to the current sense signal. The amount of added ramp is optimised and varies with the operating duty cycle. Larger duty ratios result in larger ramps being added to the current sense signal. Note that the uncorrected current signal is used for overcurrent comparator. The current limit point is unaffected by the slope compensation.

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Application Information

COMBI-SENSE OPERATION AND CURRENT LIMIT

Effective current sensing is important for the current mode control of power convertors. Instead of using the traditional lossy resistive current sense scheme, a novel lossless Combi-Sense technique is used in SC4510. This SEMTECH proprietary technology has the advantages of

- 1) lossless current sensing,
- 2) bigger signal-to-noise ratio, and
- 3) thermal run-away prevention.

The basic structure of the Combi-Sense is shown in Fig.1. Where R_L is the equivalent resistance of the output inductor. The added R_s and C_s form the RC branch in “parallel” with the output inductor for inductor current sensing. This branch works with a small signal totem pole (Q3 and Q4) integrated in SC4510 in order to improve the signal-to-noise ratio. The base signals Vbe3 and Vbe4 are designed to closely follow the gate signals Vgs1 and Vgs2, respectively. Ideally, the leading and falling edges of the Virtual Phase Node (VPN) follow that of the Phase Node (PH) when Q1~Q4 switch in perfect synchronism.

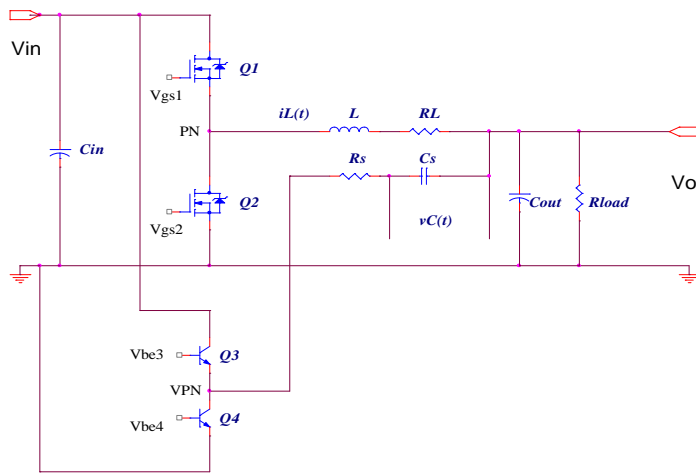


Fig.1 The Basic Structure of Combi-Sense.

When Q1/Q3 turn ON and Q2/Q4 turn OFF, the equivalent circuit of Fig.1 is shown in Fig. 2a). Where, R_{ds1} is the on-resistance of the top MOSFET. The two branches, consisting of $\{(R_{ds1}+R_L), L\}$ and $\{R_s, C_s\}$, are in parallel. The DC voltage drop $(R_{ds1}+R_L)I_o$ equals V_{cs} . In this way, the output current is sensed from V_{cs} when $(R_{ds1}+R_L)$ is known.

When Q1/Q3 turn OFF and Q2/Q4 turn ON, the equivalent circuit of Fig.1 becomes the sub-circuit as shown in Fig. 2b). Where R_{ds2} is the channel resistance of the bottom MOSFET. In this case, the branch $\{R_s, C_s\}$ is in parallel with $\{(R_{ds2}+R_L), L\}$ and $V_{cs}=(R_{ds2}+R_L)I_o$.

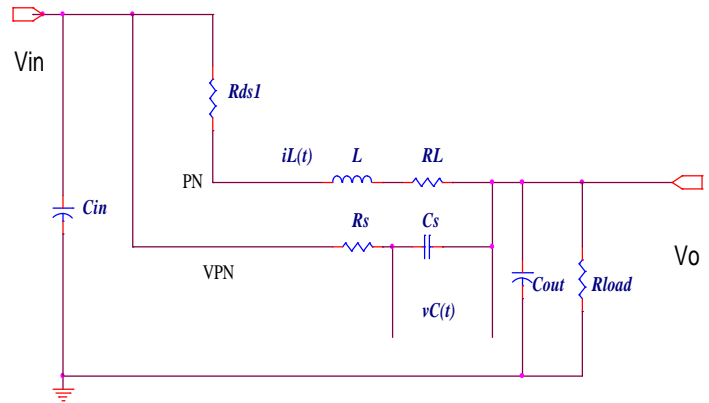


Fig.2 a) Equivalent sub-circuit.

When averaged over a complete cycle,

$$\begin{aligned}
 V_{cs} &= [D(R_{ds1}+R_L)+(1-D)(R_{ds2}+R_L)] I_o \\
 &= [D R_{ds1}+(1-D)R_{ds2}+R_L] I_o \\
 &= R_{eq} I_o.
 \end{aligned}$$

D is the operating duty ratio. It is noted that the average DC value in V_{cs} is independent of the value of L, R_s and C_s . If only the average load current information is needed (such as in average current mode control), this current sensing method is effective without further requirements.

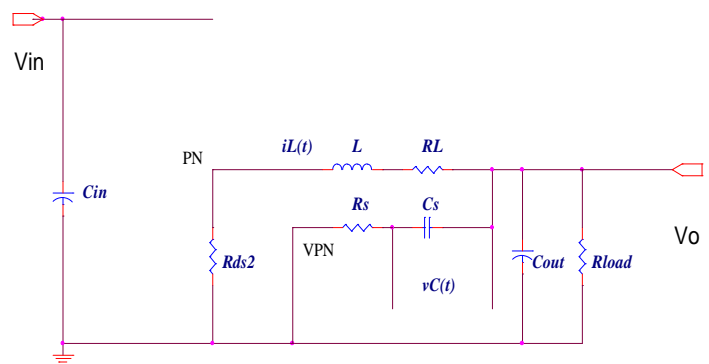


Fig.2 b) Equivalent sub-circuit.

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Application Information (Contd.)

In peak current mode control as in SC4510, the voltage ripple on C_s is critical for PWM operation. In fact, the peak-to-peak value of the voltage ripple across V_{Cs} (denoted as ΔV_{Cs}) directly affects the signal-to-noise ratio of the PWM operation. In general, smaller ΔV_{Cs} leads to small signal-to-noise ratio and more noise sensitive operation. Larger ΔV_{Cs} leads to more circuit (power stage) parameter sensitive operation. A good engineering compromise is to make

$$\Delta V_{Cs} \sim R_{eq} \Delta I_o$$

Where ΔI_o is the peak to peak ripple current in the inductor. The prerequisite for such relation is the so called time constant matching condition

$$\frac{L}{R_{eq}} \approx R_s C_s$$

When $R_{ds1} = R_{ds2}$, the above approximations become precise equalities. For the example in the Application Circuit shown on p9 the inductor value is 1 μ H,

$$RL = 1.4 \text{ m}\Omega, \quad R_{ds1} = 11 \text{ m}\Omega \quad \text{and} \quad R_{ds2} = 3 \text{ m}\Omega$$

Since the operating duty ratio is very small the effective Rds is determined mostly by Rds2. The time constant $R_s C_s$ should be set close to 0.2 mS. Since the effective value of R_s is $20 \text{ k}\Omega // 18 \text{ k}\Omega = 9.5 \text{ k}\Omega$, $C_s = 22 \text{ nF}$ was chosen.

CURRENT LIMIT SCALING

In SC4510, the current limiting is performed on cycle-by-cycle basis. When the voltage difference between CS+ and CS- exceeds 65 mV, the top MOSFET duty ratio is clipped in order to limit the output source current. Similarly, when the voltage difference between CS- and CS+ exceeds 113 mV, the bottom MOSFET duty ratio is clipped in order to limit the sink current. For the configuration in Fig.1, the convertor output current limit is set around

$$I_{LMcp} = \frac{75 \text{ mV}}{R_{eq}}$$

for the current sourcing mode and

$$I_{LMcn} = -\frac{110 \text{ mV}}{R_{eq}}$$

for the current sinking mode.

In the application circuit, $R_{eq} = 5.6 \text{ m}\Omega$. However the peak value of the sensed current is not exact for a number of reasons. Though the Phase Node PH and Virtual Phase Node VPN voltages are assumed to be identical, there will be some offset between them which adds to the average value of the current feedback signal. This is particularly true during the switching transitions where rise and fall times of the true Phase Node are dependent on the power MOSFET characteristics. The peak value of the signal also includes the ripple current ΔI_o riding on the output DC current. In addition, the signal level is subject to variations with respect to input and PVCC voltages. The difference between sensed current magnitude and the actual current gets more pronounced for low output voltages where the operating duty is also low.

Given these differences, some amount of scaling the current sense signal is required to adjust the current limit in most applications. This can be accomplished easily by simple resistor networks and the possible configurations are shown in Fig.3.

a) When the required current limit value I_{LM} is greater than I_{LMcp} , remove R_{s3} and solve for for $R_{s2} = R_{seq}$ and

$$R_{seq} C_s = \frac{L}{R_{eq}}$$

R_{seq} is the parallel combination of R_s and R_{s1} as shown in Fig 3). R_{s2} helps to reduce the offset at the input of current sense amplifier inside SC4510.

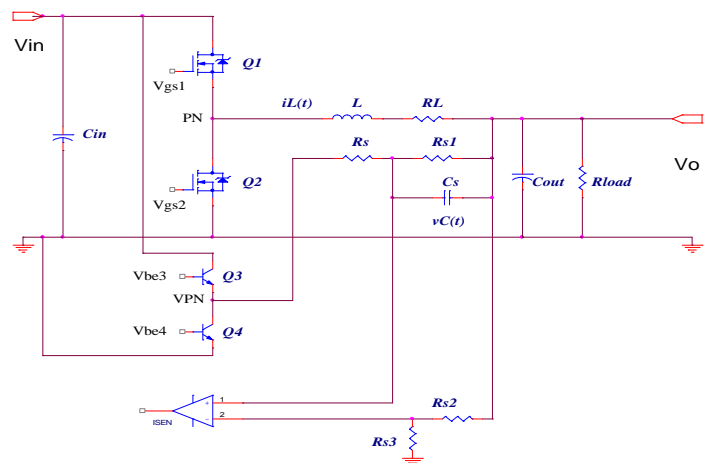


Fig.3 Current limit scaling.

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Application Information (Contd.)

For simplicity R_{s2} can be omitted and the current limit can be estimated from

$$I_{LM} R_{eq} = 75 \text{ mV} \times \frac{R_s + R_{s1}}{R_{s1}}$$

In the application circuit the current feedback signal had to be halved to account for variations explained above and ensure that the current limit is at least 20% above nominal at minimum input.

b) When the required current limit value I_{LM} is less than I_{LMcp} remove R_{s1} solve

$$R_s C_s = \frac{L}{R_{eq}}$$

for R_s and solve

$$I_{LM} R_{eq} + \frac{R_s}{R_{s3}} V_o = 75 \text{ mV}$$

to set the current limit.

Similar steps and equations apply to the current limit setting and scaling for current sinking mode.

OVERCURRENT PROTECTION AND HICCUP MODE

In addition to the current limit capability, SC4510 provides overcurrent protection in case the convertor output is shorted to ground. If this fault condition happens, the controller senses the output voltage via voltage feedback pin IN-. When the sensed voltage is below 70% of the normal feedback voltage, the controller shuts down both top and bottom MOSFETs. At the same time, a current sink of 1 μ A discharges the soft start capacitor C_{SS} connected to the SS/EN pin.

When the capacitor is discharged until its voltage reaches 0.4V, the controller initiates the soft start process. If the short circuit fault persists, the controller shuts down the convertor again when the voltage across the soft start capacitor reaches 3.4V. This hiccup process repeats until the fault condition is removed. Under this situation, it is important to make sure that the convertor does not fail. One important parameter is the convertor thermal condition which is directly related to the effective inductor and MOSFETs current. The effective currents in inductor and MOSFETs can be estimated using the following equations.

a) The time it takes to discharge the capacitor from 3.4V to 0.4V

$$t_{ssf} = C_{SS} \times \frac{(3.4 - 0.4)V}{1 \text{ mA}}$$

In the application circuit, $C_{SS} = 47 \text{ nF}$ and t_{ssf} is calculated as 140 mS.

b) The time interval of the soft start process from 0.4V to 3.4V

$$t_{ssr} = C_{SS} \times \frac{(3.4 - 0.4)V}{2 \text{ mA}}$$

When $C_{SS} = 47 \text{ nF}$, t_{ssr} is calculated as 70 mS.

Notice that during the soft start process, the convertor only starts switching when the voltage at SS/EN exceeds 1.3V. Then,

c) The effective operation time interval

$$t_{sso} = C_{SS} \times \frac{(3.4 - 1.3)V}{2 \text{ mA}}$$

This is the interval where the gate drive outputs are active and current builds up in the inductor.

The effective inductor current is then

$$I_{Leff} = I_{LMcp} \frac{t_{sso}}{t_{ssf} + t_{ssr}}$$

It turns out that I_{Leff} is independent of the soft start capacitor value and is determined as $0.3I_{LMcp}$. This should lead to a reasonable thermal condition in the convertor hiccup operation. Note that I_{Leff} calculated is not the true average value of the inductor current since the convertor is still in the soft start mode during the t_{sso} interval.

POWER MANAGEMENT**Application Information (Contd.)**

PCB LAYOUT FOR SC4510

Careful attention to layout requirements is necessary for successful implementation of the SC4510 PWM controller. High switching currents with fast rise and fall times are present in the application and their effect on ground plane voltage differentials must be understood and minimized. A good layout with minimum parasitic loop areas will

- a) reduce EMI
- b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and
- c) minimize source ringing, resulting in more reliable gate switching signals.

LAYOUT GUIDELINES

In the following Q_T and Q_B denote the high side and low side MOSFETs respectively.

- 1) A ground plane should be used. The number and position of ground plane interruptions should be minimised so as not to compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents into particular paths, such as the output capacitor or the Q_B source.
- 2) The high power, high current parts of the circuit should be laid out first. The on time loop formed by the input capacitor C_{in} , the high side FET Q_T , the output inductor and the output capacitor bank C_{out} must be kept as small as possible. Another loop area to minimise is formed by low side FET Q_B , the output inductor and the output capacitor bank C_{out} during the off period. These loops contain all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance.
- 3) The connection between the junction of Q_T , Q_B and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short. The top FET gate charge currents flow in this trace.
- 4) The output capacitor C_{out} should be located as close to the load terminals as possible. Fast transient load currents are supplied by C_{out} and connections between C_{out} and the load must be kept short with wide copper areas to minimize inductance and resistance. This will improve the transient response to step loads.

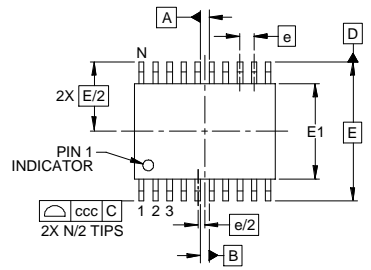
5) The SC4510 is best placed over a quiet ground plane area. Avoid pulse currents of the C_{in} , Q_T , Q_B loop flowing in this area. This analog ground plane should be connected to the power ground plane at a “quiet” point near the input capacitor. Under no circumstance should it be returned to a point inside the C_{in} , Q_T , Q_B , C_{out} power ground loops.

6) The SC4510 AGND pin is connected to the separate analog ground plane with minimum lead length. All analog grounding paths including decoupling capacitors, feedback resistors, compensation components, soft start capacitor, frequency and current-limit setting resistors should be connected to the same plane.

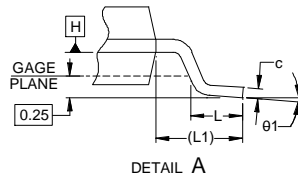
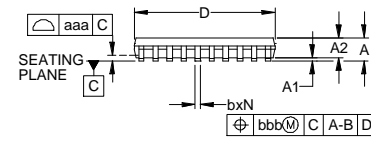
7) Locate the critical filtering capacitors as close as possible to their respective device. This is particularly true for the current feedback filtering capacitor connected between $CS+$ and $CS-$. A high value ceramic capacitor is also recommended between $PVCC$ and $PGND$ pins close to the device.

POWER MANAGEMENT

Outline Drawing - TSSOP-20

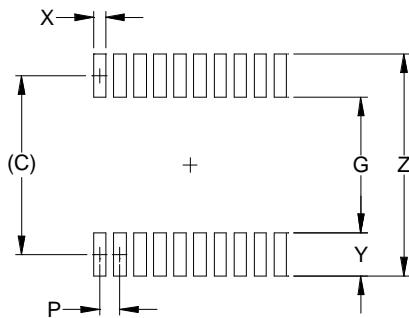


DIM	INCHES		MILLIMETERS	
	MIN	NOM MAX	MIN	NOM MAX
A	-	.047	-	1.20
A1	.002	.006	0.05	0.15
A2	.031	.042	0.80	1.05
b	.007	.012	0.19	0.30
c	.003	.007	0.09	0.20
D	.251 .255	.259	6.40 6.50	6.60
E1	.169 .173	.177	4.30 4.40	4.50
E	.252 BSC		6.40 BSC	
e	.026 BSC		0.65 BSC	
L	.018 .024	.030	0.45 0.60	0.75
L1	(0.039)		(1.0)	
N	20		20	
θ1	0°	8°	0°	8°
aaa	.004		0.10	
bbb	.004		0.10	
ccc	.008		0.20	



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS $\{-A\}$ AND $\{-B\}$ TO BE DETERMINED AT DATUM PLANE $\{H\}$.
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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