

POWER MANAGEMENT

Description

The SC431L is a three terminal adjustable shunt regulator with thermal stability guaranteed over temperature. The output voltage can be adjusted to any value from 1.24V (V_{REF}) to 20V with two external resistors. The SC431L has a typical dynamic output impedance of 0.05Ω. Active output circuitry provides a very sharp turn on characteristic, making the SC431L an excellent replacement for zener diodes.

The SC431L shunt regulator is available with four voltage tolerances (0.25%, 0.5%, 1.0% and 2.0%), two operating temperature ranges (commercial and industrial) and two package options (SOT-23-3 and SOT-23-5). This allows the designer the opportunity to select the optimum combination of cost and performance for their application.

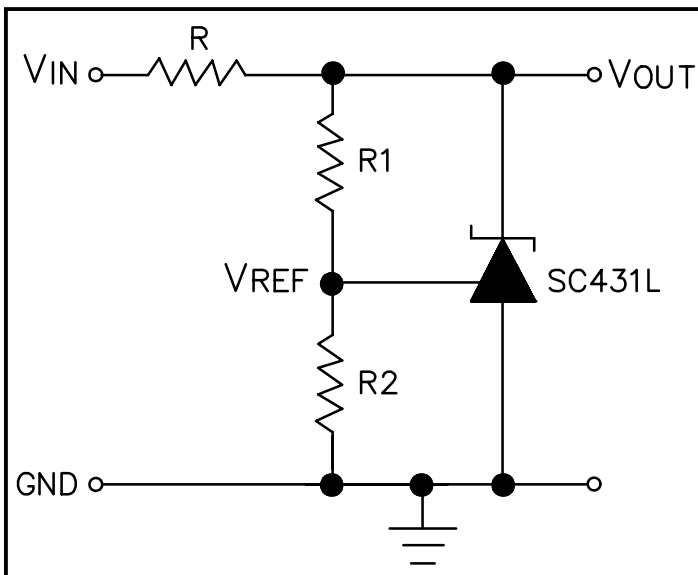
Features

- ◆ Low voltage operation (down to 1.24V)
- ◆ Wide operating current range 100μA to 100mA
- ◆ Low dynamic output impedance 0.05 Ω typ.
- ◆ Trimmed bandgap design ± 0.25%
- ◆ Upgrade for TLV431A
- ◆ SOT-23-3 and SOT-23-5 packages. Also available in Lead-free package, fully WEEE and RoHS compliant

Applications

- ◆ Linear Regulators
- ◆ Adjustable Supplies
- ◆ Switching Power Supplies
- ◆ Battery Operated Computers
- ◆ Instrumentation
- ◆ Computer Disk Drives

Typical Application Circuit⁽¹⁾⁽²⁾



Notes:

- 1) Set V_{OUT} according to the following equation:

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2} \right) + I_{REF} R1$$

- 2) Choose the value for R as follows:

- The maximum limit for R should be such that the cathode current, I_z , is greater than the minimum operating current (100μA) at $V_{IN(MIN)}$.

- The minimum limit for R should be such that I_z does not exceed 100mA under all load conditions, and the instantaneous turn-on value for I_z does not exceed 150mA. Both of the following conditions must be met:

$$R_{min} \geq \frac{V_{IN(max)}}{150 \text{ mA}} \quad (\text{to limit instantaneous turn-on } I_z)$$

$$R_{min} \geq \frac{V_{IN(max)} - V_{OUT}}{I_{OUT(min)} + 100 \text{ mA}} \quad (\text{to limit } I_z \text{ under normal operating conditions})$$

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Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
Cathode Voltage	V_Z	20	V
Continuous Cathode Current	I_Z	100	mA
Reference Input Current	I_{REF}	3	mA
Power Dissipation at $T_A = 25^\circ\text{C}$ SOT-23-3 SOT-23-5	P_D	0.37 0.49	W
Thermal Resistance SOT-23-3 SOT-23-5	θ_{JA}	336 256	$^\circ\text{C/W}$
Operating Ambient Temperature Range SC431LC SC431LI	T_A	0 to +70 -40 to +85	$^\circ\text{C}$
Operating Junction Temperature Range SC431LC SC431LI	T_J	0 to +150 -40 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 to +150	$^\circ\text{C}$
Lead Temperature (Soldering) 10 seconds	T_{LEAD}	300	$^\circ\text{C}$
ESD Rating (Human Body Model)	V_{ESD}	2	kV

Electrical Characteristics

Unless specified: $T_A = 25^\circ\text{C}$. Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Condition	SC431L 0.25%			SC431L 0.5%			Units
			Min	Typ	Max	Min	Typ	Max	
Reference Voltage	V_{REF}	$V_Z = V_{REF}, I_Z = 10\text{mA}^{(1)}$	1.237 1.224	1.240	1.243 1.256	1.234 1.222	1.240	1.246 1.258	V
V_{REF} Temp Deviation	V_{DEV}	$V_Z = V_{REF}, I_Z = 10\text{mA}^{(1)}$		10	25		10	25	mV
Ratio of Change in V_{REF} to Change in V_Z	$\frac{\Delta V_{REF}}{\Delta V_Z}$	$I_Z = 10\text{mA}, \Delta V_Z = 16\text{V to } V_{REF}$		-1.0	-2.7		-1.0	-2.7	mV/V
Reference Input Current	I_{REF}	$R1 = 10\text{k}\Omega, R2 = \infty, I_Z = 10\text{mA}^{(2)}$		0.15	0.5		0.15	0.5	μA
I_{REF} Temperature Deviation	$I_{REF(DEV)}$	$R1 = 10\text{k}\Omega, R2 = \infty, I_Z = 10\text{mA}^{(2)}$		0.1	0.4		0.1	0.4	μA
Off-State Cathode Current	$I_{Z(OFF)}$	$V_{REF} = 0\text{V}, V_Z = 6\text{V}^{(3)}$ $V_{REF} = 0\text{V}, V_Z = 16\text{V}^{(3)}$		0.125 0.135	0.150		0.125 0.135	0.150	μA

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Electrical Characteristics (Cont.)

 Unless specified: $T_A = 25^\circ\text{C}$. Values in **bold** apply over full operating ambient temperature range.

(Continued from page 2)			SC431L 0.25%			SC431L 0.5%			
Parameter	Symbol	Condition	Min	Typ	Max	Min	Typ	Max	Units
Dynamic Output Impedance	r_z	$f < 1\text{kHz}, V_Z = V_{REF}$ $I_Z = 100\mu\text{A to } 100\text{mA}^{(1)}$		0.05	0.15		0.05	0.15	Ω
Minimum Operating Current	$I_{Z(MIN)}$	$V_Z = V_{REF}^{(1)}$		20	100		20	100	μA

			SC431L 1%			SC431L 2%			
Parameter	Symbol	Condition	Min	Typ	Max	Min	Typ	Max	Units
Reference Voltage	V_{REF}	$V_Z = V_{REF}, I_Z = 10\text{mA}^{(1)}$	1.228 1.215	1.240	1.252 1.265	1.215 1.200	1.240	1.265 1.280	V
V_{REF} Temp Deviation	V_{DEV}	$V_Z = V_{REF}, I_Z = 10\text{mA}^{(1)}$		10	25		10	35	mV
Ratio of Change in V_{REF} to Change in V_Z	$\frac{\Delta V_{REF}}{\Delta V_Z}$	$I_Z = 10\text{mA}, \Delta V_Z = 16\text{V to } V_{REF}$		-1.0	-2.7		-1.0	-2.7	mV/V
Reference Input Current	I_{REF}	$R1 = 10\text{k}\Omega, R2 = \infty,$ $I_Z = 10\text{mA}^{(2)}$		0.15	0.5		0.15	0.5	μA
I_{REF} Temperature Deviation	$I_{REF(DEV)}$	$R1 = 10\text{k}\Omega, R2 = \infty,$ $I_Z = 10\text{mA}^{(2)}$		0.1	0.4		0.1	0.4	μA
Off-State Cathode Current	$I_{Z(OFF)}$	$V_{REF} = 0\text{V}, V_Z = 6\text{V}^{(3)}$ $V_{REF} = 0\text{V}, V_Z = 16\text{V}^{(3)}$		0.125 0.135	0.150		0.125 0.135	0.150	μA
Dynamic Output Impedance	r_z	$f < 1\text{kHz}, V_Z = V_{REF}$ $I_Z = 100\mu\text{A to } 100\text{mA}^{(1)}$		0.05	0.15		0.05	0.15	Ω
Minimum Operating Current	$I_{Z(MIN)}$	$V_Z = V_{REF}^{(1)}$		20	100		20	100	μA

Notes:

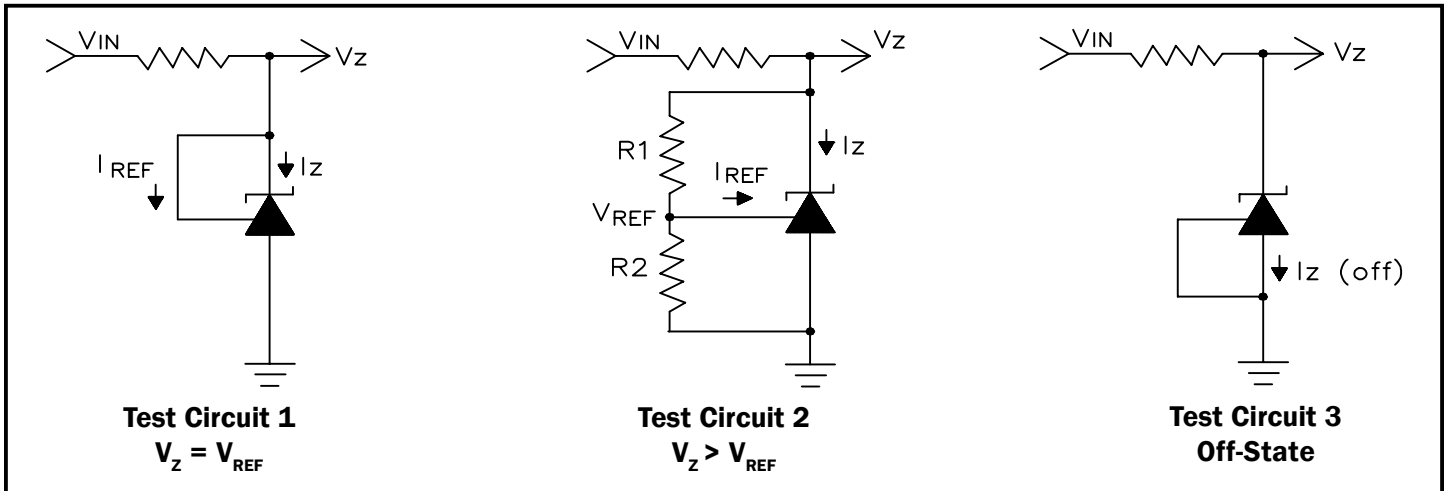
- (1) See Test Circuit 1 on page 4.
- (2) See Test Circuit 2 on page 4.
- (3) See Test Circuit 3 on page 4.

Recommended Operating Conditions

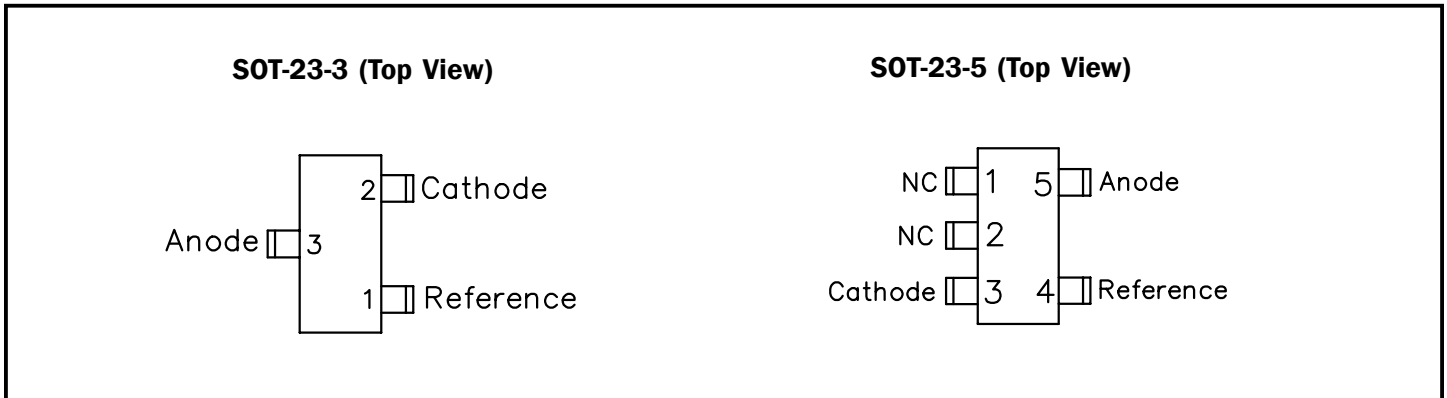
	Min	Max	Symbol
Cathode Voltage, V_Z	V_{REF}	16	V
Cathode Current, I_Z	100 μA	100	mA

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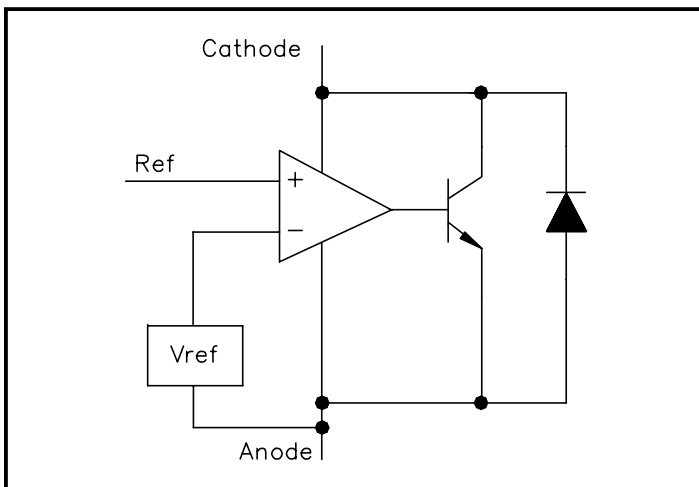
Test Circuits



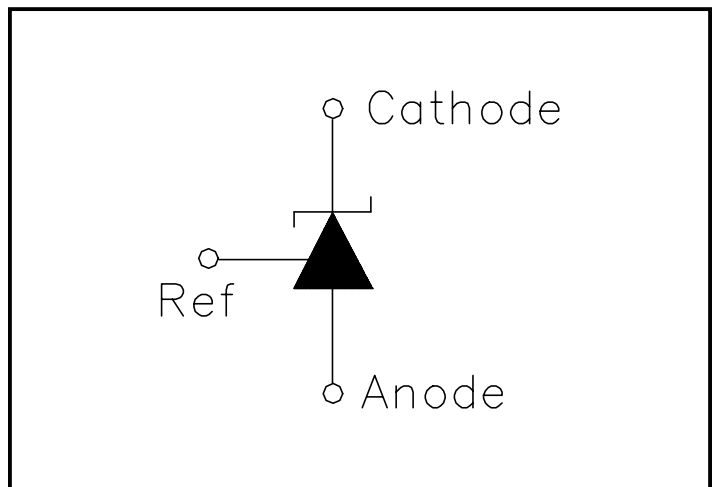
Pin Configurations



Block Diagram



Symbol



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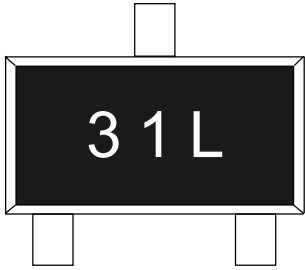
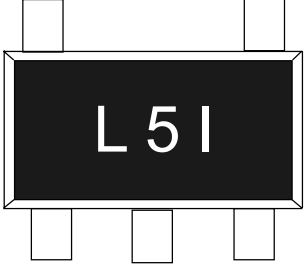
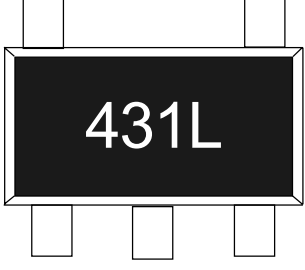
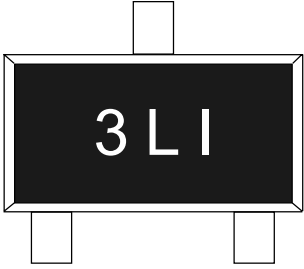
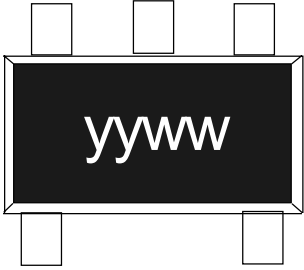
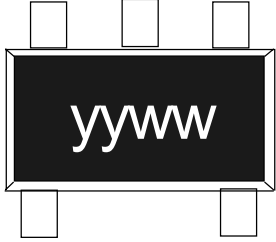
Ordering Information

Package	T _j (°C)	Tolerance			
		0.25%	0.5%	1.0%	2.0%
SOT-23-3 ⁽¹⁾⁽²⁾	0 to +150	SC431LCSK-.25TR	SC431LCSK-.5TR	SC431LCSK-1TR	SC431LCSK-2TR
		SC431LCSK-25TRT	SC431LCSK-.5TRT	SC431LCSK-1TRT	SC431LCSK-2TRT
	-40 to +150	SC431LISK-.25TR	SC431LISK-.5TR	SC431LISK-1TR	SC431LISK-2TR
		SC431LISK-.25TRT	SC431LISK-.5TRT	SC431LISK-1TRT	SC431LISK-2TRT
SOT-23-5 ⁽¹⁾⁽²⁾	0 to +150	SC431LC5SK.25TR	SC431LC5SK-.5TR	SC431LC5SK-1TR	SC431LC5SK-2TR
		SC431LC5SK25TRT	SC431LC5SK.5TRT	SC431LC5SK-1TRT	SC431LC5SK-2TRT
	-40 to +150	SC431LI5SK.25TR	SC431LI5SK-.5TR	SC431LI5SK-1TR	SC431LI5SK-2TR
		SC431LI5SK25TRT	SC431LI5SK.5TRT	SC431LI5SK-1TRT	SC431LI5SK-2TRT

Notes:

- (1) Only available in tape and reel packaging. A reel contains 3000 devices.
- (2) "T" at end of part number indicates "lead free". This product is fully WEEE and RoHS compliant.

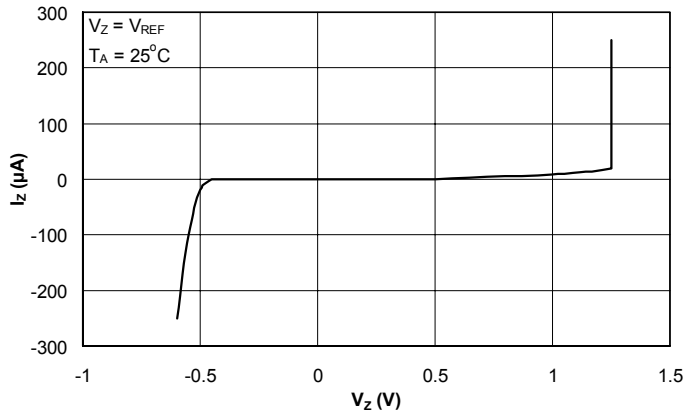
Marking Information

<p>SOT-23-3 (Top View only) (0 to +150°C)</p> 	<p>SOT-23-5 (Top View) (-40 to +150°C)</p> 	<p>SOT-23-5 (Top View) (0 to +150°C)</p> 
<p>SOT-23-3 (Top View only) (-40 to +150°C)</p> 	<p>SOT-23-5 (Bottom View)</p>  <p>yyww = Datecode, Example: (0115)</p>	<p>SOT-23-5 (Bottom View)</p>  <p>yyww = Datecode, Example: (0015)</p>

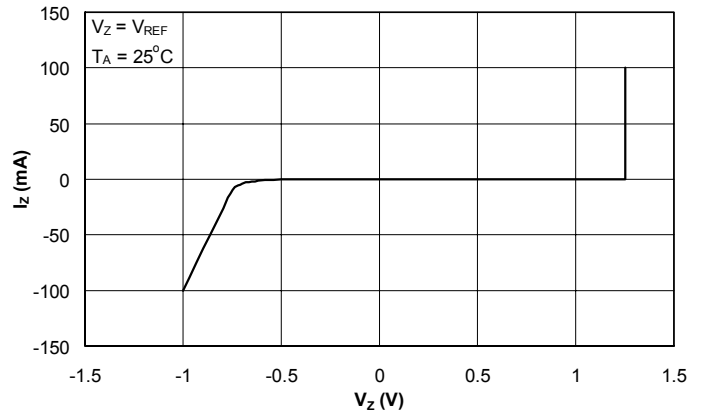
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Typical Characteristics

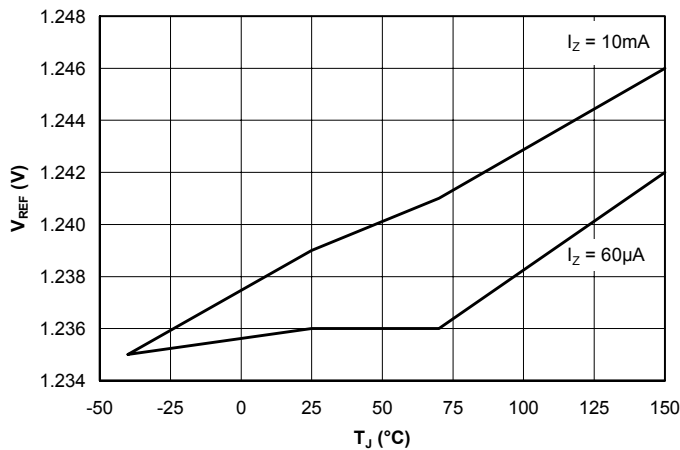
**Cathode Current vs.
Cathode Voltage**



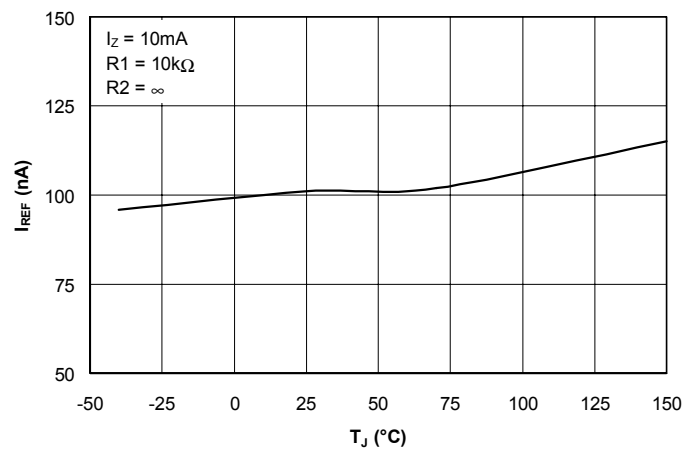
**Cathode Current vs.
Cathode Voltage**



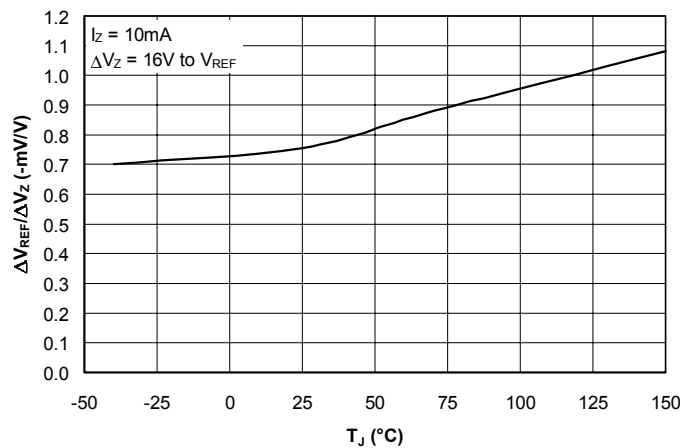
**Reference Voltage vs.
Junction Temperature**



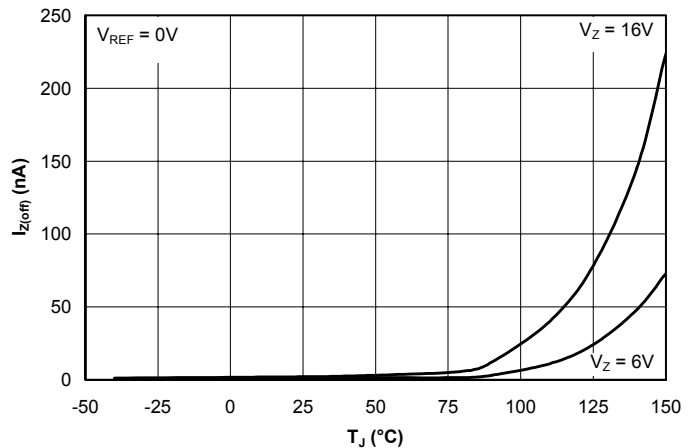
**Reference Input Current vs.
Junction Temperature**



**Ratio of Delta Reference Voltage to Delta Cathode
Voltage vs. Junction Temperature**



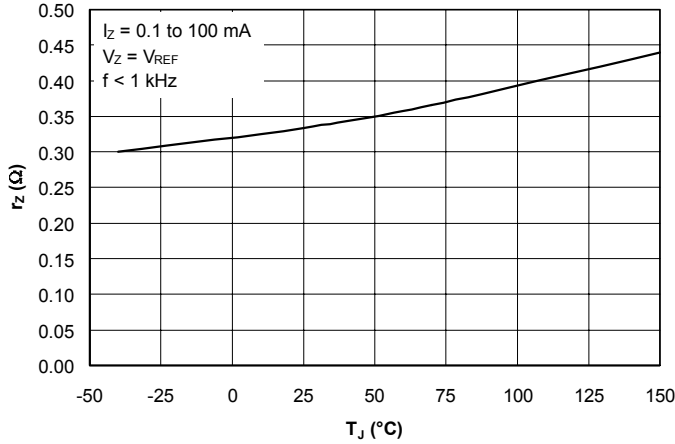
**Off-State Cathode Current
vs. Junction Temperature**



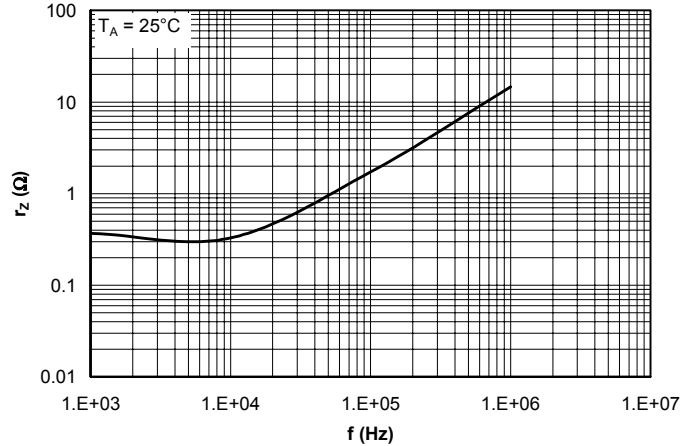
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Typical Characteristics (Cont.)

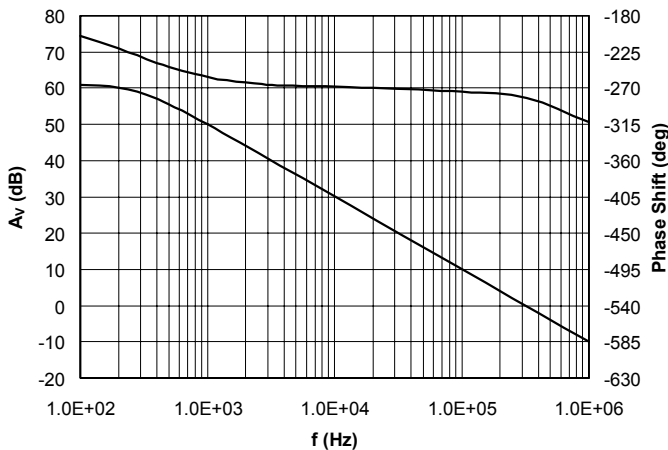
Reference Impedance vs. Junction Temperature



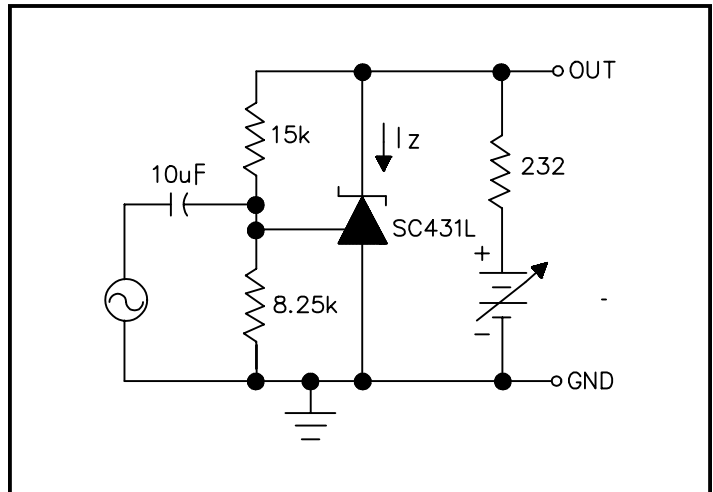
Reference Impedance vs. Frequency



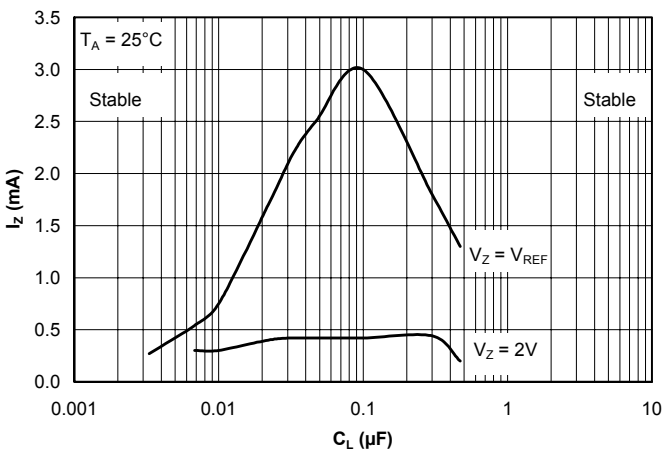
Small-Signal Gain and Phase Shift vs. Frequency



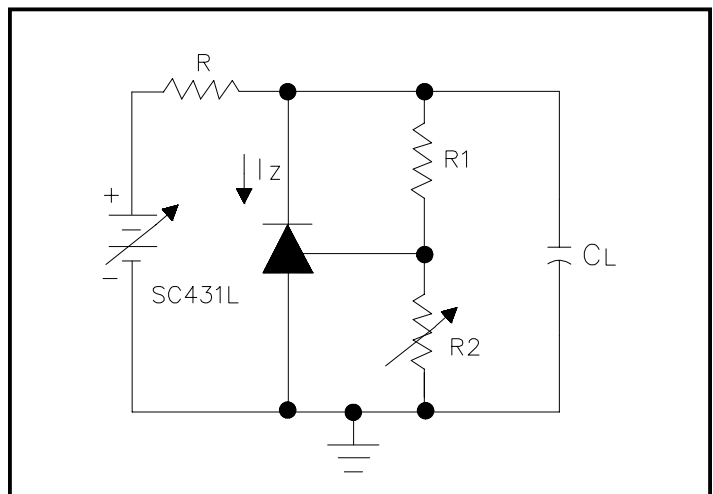
Test Circuit - Small-Signal Gain and Phase



Stability Boundary Condition For Shunt Regulation vs. Cathode Current and Load Capacitance



Test Circuit - Stability



POWER MANAGEMENT**Applications Information - Stability****Selection of load capacitance when using SC431L as a shunt regulator**

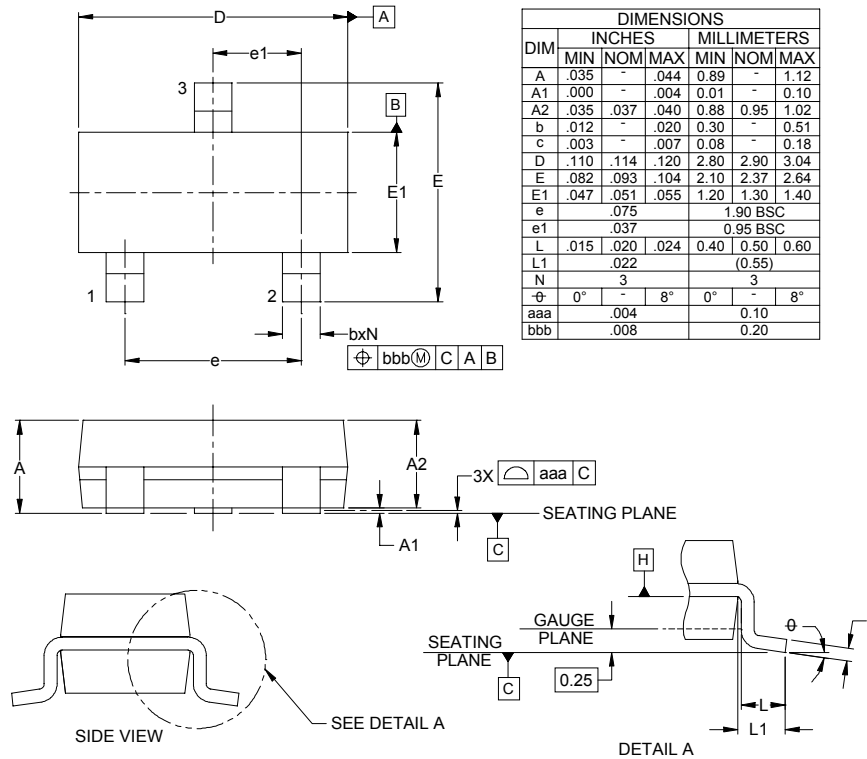
When the SC431L is used as a shunt regulator, two options for selection of C_L (see diagram on page 7) are recommended for optimal stability:

- 1) No load capacitance across the device, decouple at the load.
- 2) Large capacitance across the device, optional decoupling at the load.

The reason for this is that SC431L exhibits instability with capacitances in the range of 10nF to 1 μ F (approx.) at light cathode currents (up to 3mA typical). The device is less stable the lower the cathode voltage has been set for. Therefore while the device will be perfectly stable operating at a cathode current of (say) 10mA with a 0.1 μ F capacitor across it, it will oscillate transiently during start-up as the cathode current passes through the instability region. Selecting a very low (or preferably, no) capacitance, or alternatively a high capacitance (such as 10 μ F) will avoid this issue altogether. Since the user will probably wish to have local decoupling at the load anyway, the most cost effective method is to use no capacitance at all directly across the device. PCB trace/via resistance and inductance prevent the local load decoupling from causing the oscillation during the transient start-up phase. Note: if the SC431L is located right at the load, so the load decoupling capacitor is directly across it, then this capacitor will have to be ≤ 1 nF or $\geq 10\mu$ F.

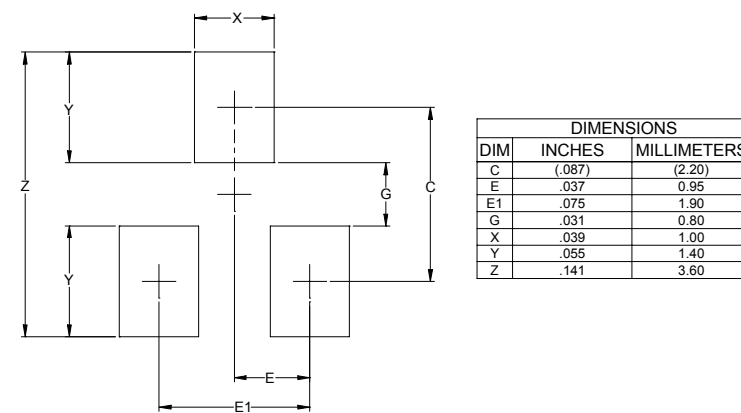
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Outline Drawing - SOT-23-3



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT-23-3



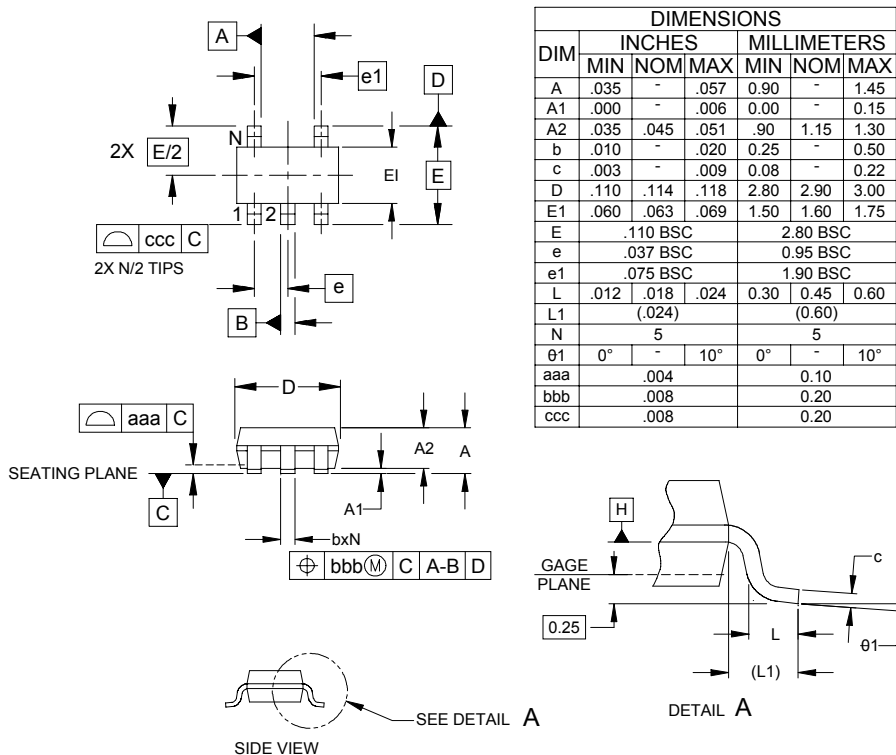
- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
 2. REFERENCE IPC-SM-782A.

Note:

(1) Grid placement courtyard is 8 x 8 elements (4mm x 4mm) in accordance with the international grid detailed in IEC Publication 97.

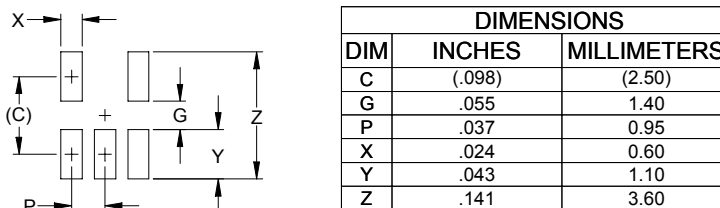
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Outline Drawing - SOT-23-5



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT-23-5



- NOTES:
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