10A EcoSpeed™ Integrated FET Regulator with Programmable LDO

POWER MANAGEMENT

Features

- Power system:
  - Input voltage — 3V to 28V
  - Integrated bootstrap switch
  - Programmable LDO output — 200mA
  - 1% reference tolerance -40 to +85 °C
  - Selectable internal/external bias power supply
  - EcoSpeed™ architecture with pseudo-fixed frequency adaptive on-time control
- Logic input/output control
  - Independent control EN for LDO and switcher
  - Programmable V_{IN} UVLO threshold
  - Power good output
  - Selectable ultrasonic/power save methods
- Protections
  - Over-voltage/under-voltage
  - TC compensated $R_{DS(ON)}$ sensed current limit
  - Thermal shutdown
- Output capacitor types
  - High ESR — SP, POSCAP, OSCON
  - Ceramic capacitors
- Package — 5x5mm, 32-pin MLPQ
- Lead-free and halogen free
- RoHS and WEEE compliant

Applications

- Office automation and computing
- Networking and telecommunication equipment
- Point-of-load power supplies and module replacement.

Description

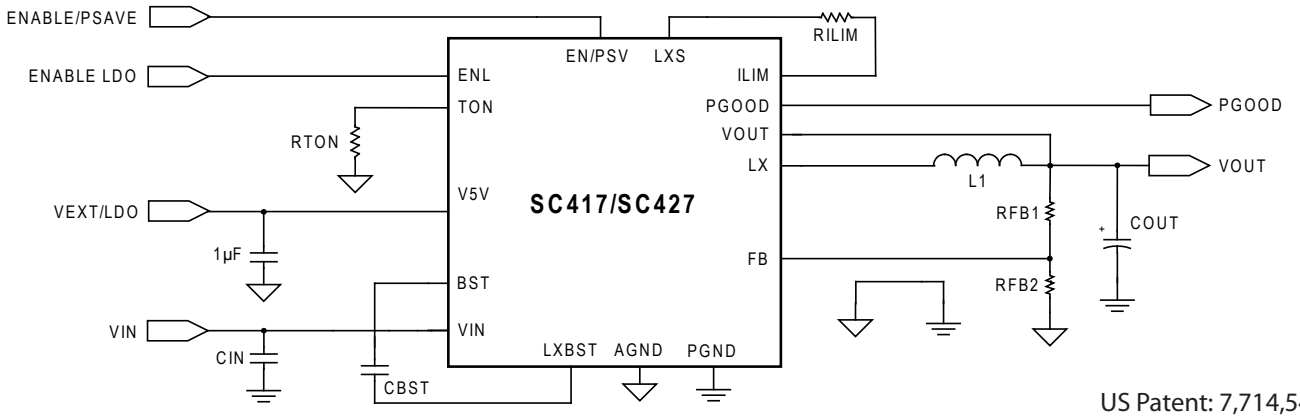
The SC417/SC427 is a stand-alone synchronous EcoSpeed™ buck regulator which incorporates Semtech's advanced, patented adaptive on-time control architecture to provide excellent light-load efficiency and fast transient response. It features integrated power MOSFETs, a bootstrap switch, and a programmable LDO in a 5x5mm package. The device is highly efficient and uses minimal 15x20mm PCB area for a total converter solution. Refer to page 16 for information on the C-SIM simulation tool.

The SC417/SC427 supports using standard capacitor types such as electrolytic or special polymer, in addition to ceramic, at switching frequencies up to 1MHz. The programmable frequency, synchronous operation, and selectable power-save provide high efficiency operation over a wide load range. In power-save mode, the minimum operating frequency for the SC417 is 25kHz whereas the SC427 has no minimum.

Additional features include internal soft-start, programmable cycle-by-cycle over-current limit protection, under and over-voltage protections and soft shutdown. The device also provides separate enable inputs for the PWM controller and LDO as well as a power good output for the PWM controller.

The wide input voltage range, programmable frequency, and programmable LDO make the device extremely flexible and easy to use in a broad range of applications. Support is provided for single cell or multi-cell battery systems in addition to traditional DC power supply applications.

Typical Application Circuit



US Patent: 7,714,547 B2

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Absolute Maximum Ratings

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns max.) ..... -2 to +30
VIN to PGND (V) ..... -0.3 to +30
EN/PSV, PGOOD, ILIM, to GND (V) ..... -0.3 to +(V5V+0.3)
VOUT, VLDO, FB, FBL, to GND (V) ..... -0.3 to +(V5V+0.3)
V5V to PGND (V) ..... -0.3 to +6
TON to PGND (V) ..... -0.3 to +(V5V - 1.5)
ENL (V) ..... -0.3 to V_{IN}
BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +35
AGND to PGND (V) ..... -0.3 to +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
V5V to PGND (V) ..... 4.5 to 5.5
VOUT to PGND (V) ..... 0.5 to 5.5

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient [2] (°C/W)
- High-side MOSFET 25
- Low-side MOSFET 20
- PWM controller and LDO thermal resistance 50

Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, V5V = +5V, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
Input Supply Voltage		3		28	V
V5V Voltage		4.5		5.5	V
VIN UVLO Threshold[1]	Sensed at ENL pin, rising edge	2.40	2.60	2.95	V
	Sensed at ENL pin, falling edge	2.23	2.40	2.57	
VIN UVLO Hysteresis	EN/PSV = High		0.2		V
V5V UVLO Threshold	Measured at V5V pin, rising edge	3.7	3.9	4.1	V
	Measured at V5V pin, falling edge	3.5	3.6	3.75	
V5V UVLO Hysteresis			0.3		V
VIN Supply Current	ENL , EN/PSV = 0V, V_{IN} = 28V		8.5	20	µA
	Standby mode; ENL=V5V, EN/PSV = 0V		130		

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Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
V5V Supply Current	ENL , EN/PSV = 0V		3	7	µA
	SC417, EN/PSV = V5V, no load (f_{SW} = 25kHz), V_{FB} > 500mV(2)		2		mA
	SC427, EN/PSV = V5V, no load, V_{FB} > 500mV(2)		0.7		
	f_{SW} = 250kHz, EN/PSV = floating , no load(2)		10		
FB On-Time Threshold	Static V_{IN} and load, 0 to +85 °C	0.496	0.500	0.504	V
	Static V_{IN} and load, -40 to +85 °C	0.495		0.505	V
Frequency Range	Continuous mode operation	200		1000	kHz
	Minimum f_{SW}, (SC417 only), EN/PSV = V5V, no load		25		
Bootstrap Switch Resistance			10		Ω
Timing					
On-Time	Continuous mode operation, V_{IN} = 15V, V_{OUT} = 5V, f_{SW}= 300kHz, R_{TON} = 133kΩ	999	1110	1220	ns
Minimum On-Time (2)			80		ns
Minimum Off-Time (2)			250		ns
Soft-Start					
Soft-Start Ramp Time (2)			850		µs
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND	-3	0	+3	mV
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal 500mV reference		+20		%
	Lower limit, V_{FB} < internal 500mV reference		-10		%
Start-Up Delay Time			2		ms
Fault (noise immunity) Delay Time(2)			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Fault Protection					
Valley Current Limit	R_{ILIM} = 5.9k Ω	6	8	10	A
I_{LIM} Source Current			10		µA
I_{LIM} Comparator Offset	With respect to AGND	-10	0	+10	mV
Output Under-Voltage Fault	V_{FB} with respect to internal 500mV reference, 8 consecutive clocks		-25		%
Smart Power-save Protection Threshold (2)	V_{FB} with respect to internal 500mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 500mV reference		+20		%
Over-Voltage Fault Delay(2)			5		µs
Over-Temperature Shutdown(2)	10°C hysteresis		150		°C
Logic Inputs/Outputs					
Logic Input High Voltage	ENL	1.0			V
Logic Input Low Voltage	ENL			0.4	V
EN/PSV Input for PSAVE Operation (2)	V5V = 5V	2.2		5	V
EN/PSV Input for Forced Continuous Operation (2)		1		2	V
EN/PSV Input for Disabling Switcher (2)				0.4	V
EN/PSV Input Bias Current	EN/PSV= V5V or AGND	-10		+10	µA
ENL Input Bias Current	V_{IN} = 28V		11	18	µA
FBL, FB Input Bias Current	FBL, FB = V5V or AGND	-1		+1	µA

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Linear Regulator (LDO)					
FBL Accuracy	VLDO load = 10mA	0.735	0.75	0.765	V
LDO Current Limit	Start-up and foldback, V_{IN} = 12V		85		mA
	Operating current limit, V_{IN} = 12V	135	200		
VLDO to VOUT Switch-over Threshold (3)		-140		+140	mV
VLDO to VOUT Non-switch-over Threshold (3)		-450		+450	mV
VLDO to VOUT Switch-over Resistance	V_{OUT} = +5V		2		Ω
LDO Drop Out Voltage (4)	From V_{IN} to V_{VLDO}, V_{VLDO} = +5V, I_{VLDO} = 100mA		1.2		V

Notes:

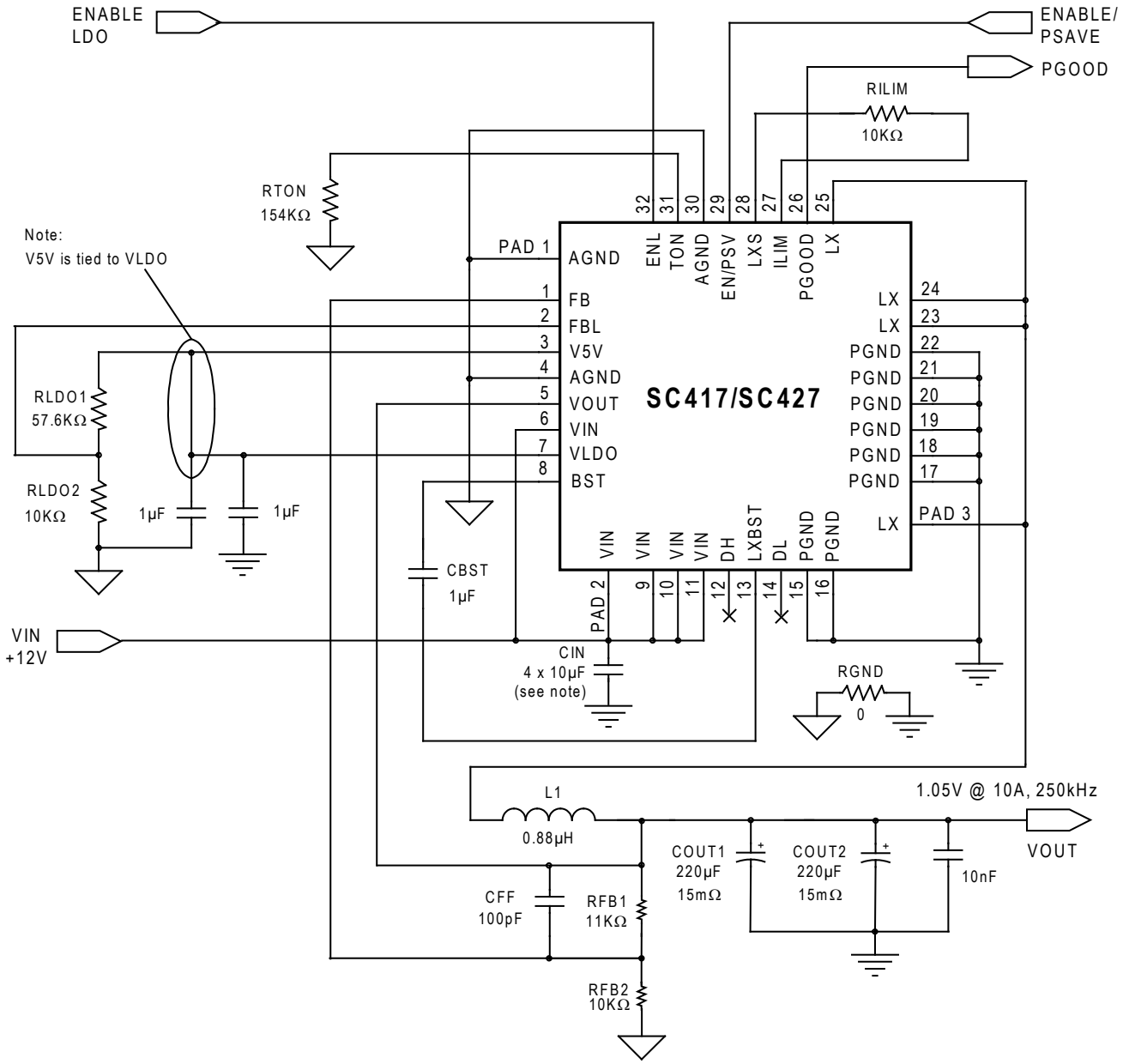
(1) V_{IN} UVLO is programmable using a resistor divider from VIN to ENL to AGND. The ENL voltage is compared to an internal reference.

(2) Guaranteed by design.

(3) The switch-over threshold is the maximum voltage differential between the VLDO and VOUT pins which ensures that VLDO will internally switch-over to VOUT. The non-switch-over threshold is the minimum voltage differential between the VLDO and VOUT pins which ensures that VLDO will not switch-over to VOUT.

(4) The LDO drop out voltage is the voltage at which the LDO output drops 2% below the nominal regulation point.

Detailed Application Circuit



Key Components

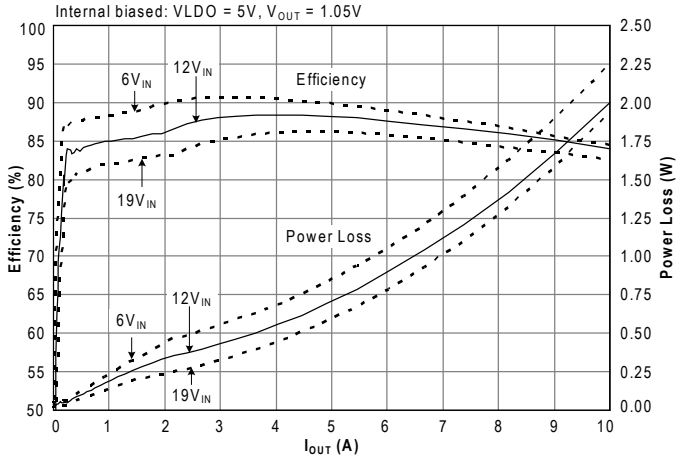
Component	Value	Manufacturer	Part Number	Web
CIN	4 x 10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT1,2 (option 1)	2 x 220µF/15mΩ	Panasonic	EEFUE0J221R	www.panasonic.com
COUT1,2 (option 2)	330µF/9mΩ	Panasonic	EEF-SX0E331ER	www.panasonic.com
L1 (option 1)	0.88µH/2.3mΩ	NEC-Tokin	MPC1040LR88C	www.nec-tokin.com
L1 (option 2)	1.0µH/2.3mΩ	Vishay	IHLP4040DZER1R0M11	www.vishay.com
All other small signal components (resistors and capacitors) are standard SMT devices.				

NOTE: The quantity of 10µF input capacitors required varies with the application requirements.

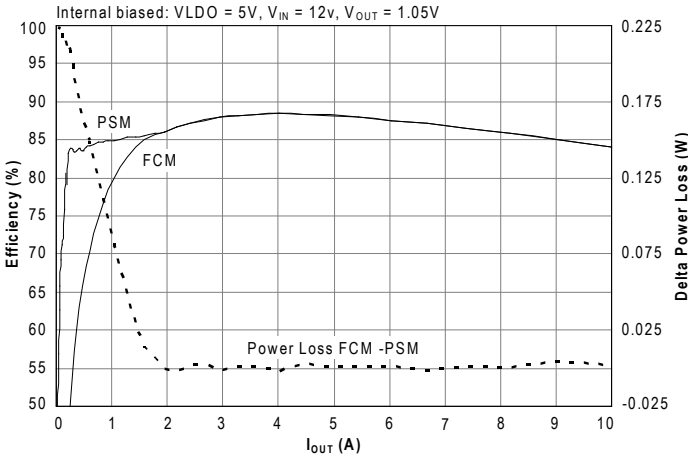
Typical Characteristics

Characteristics in this section are based on using the Detailed Application Circuit on page 7 (SC417/SC427).

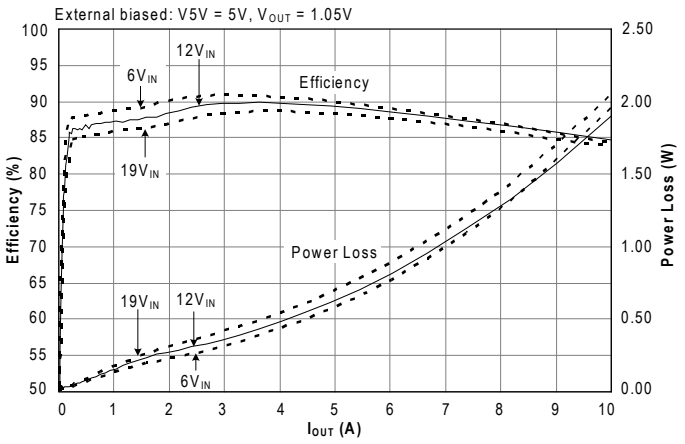
SC417 Efficiency/Power Loss vs. Load — PSAVE Mode



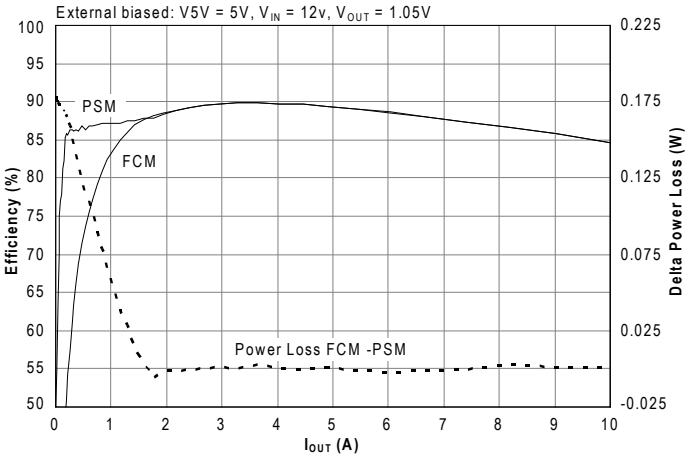
SC417 Efficiency/Power Loss — PSAVE vs. FCM



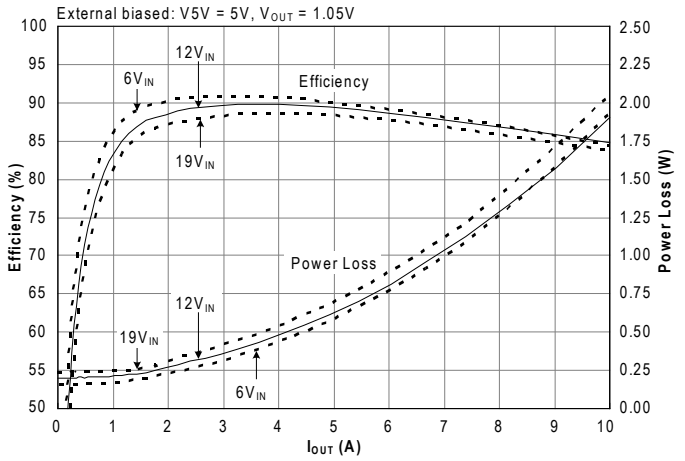
SC417 Efficiency/Power Loss vs. Load — PSAVE Mode



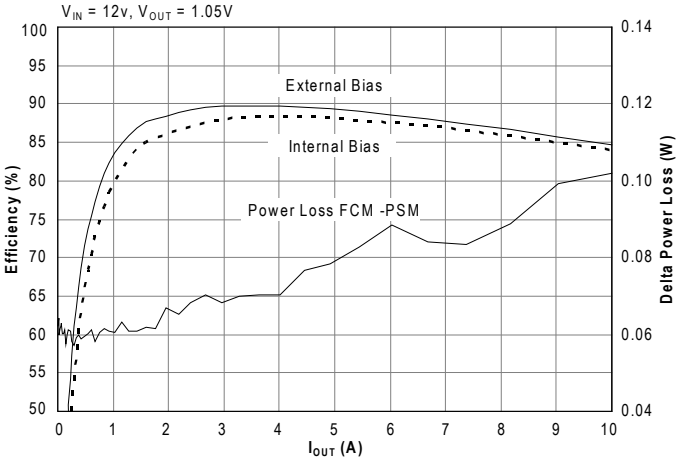
SC417 Efficiency/Power Loss — PSAVE vs. FCM



SC417 Efficiency/Power Loss vs. Load — FCM



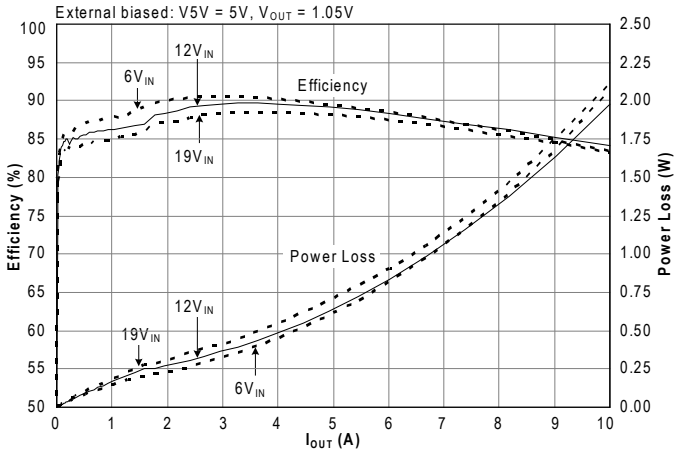
SC417 Efficiency/Power Loss — FCM



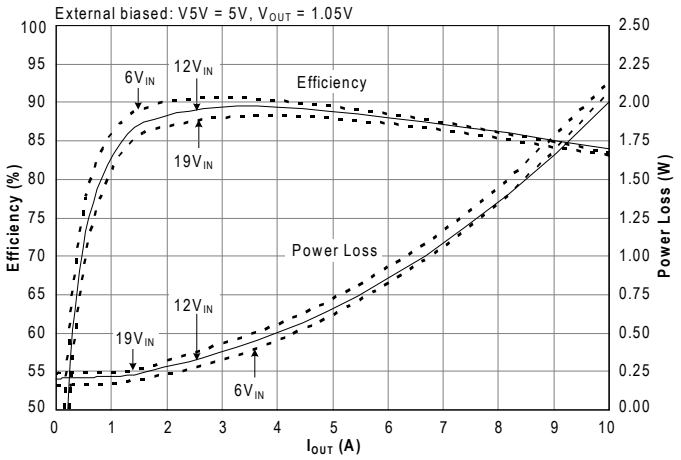
Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit on page 7 (SC417/SC427).

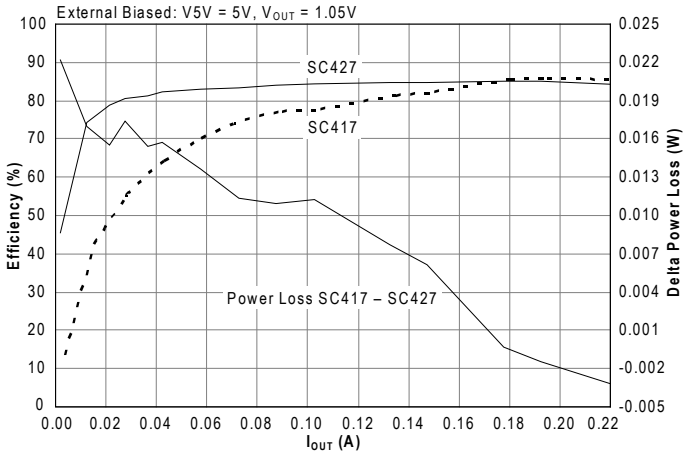
SC427 Efficiency/Power Loss vs. Load — PSAVE Mode



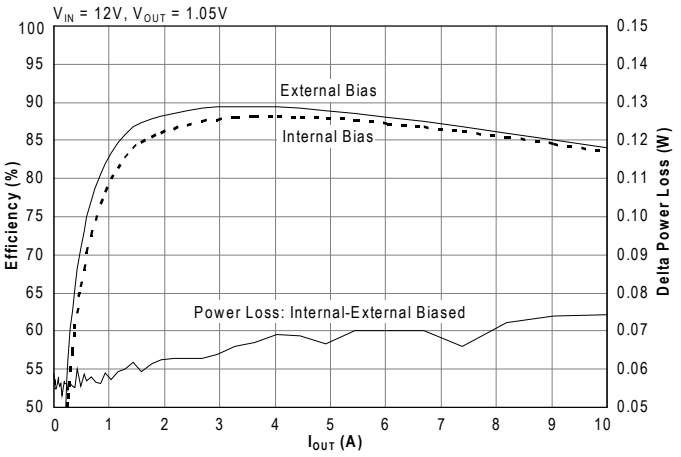
SC427 Efficiency/Power Loss vs. Load — FCM



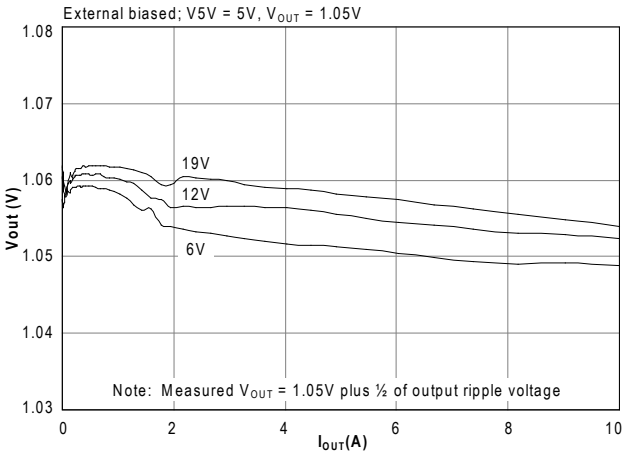
SC417 vs. SC427 Efficiency/Power Loss — PSAVE Mode



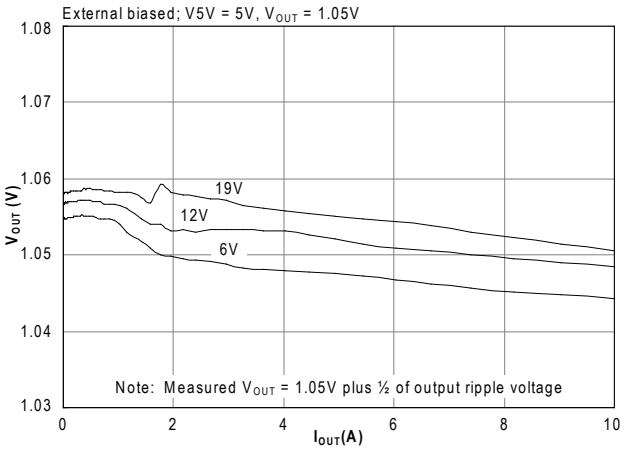
SC427 Efficiency/Power Loss — FCM



SC417 Load Regulation —PSAVE Mode



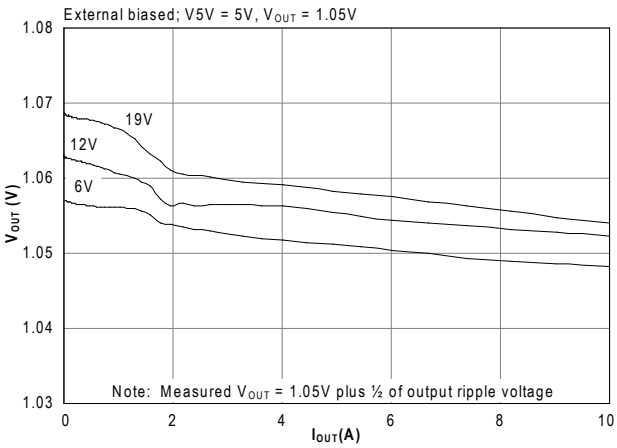
SC427 Load Regulation —PSAVE Mode



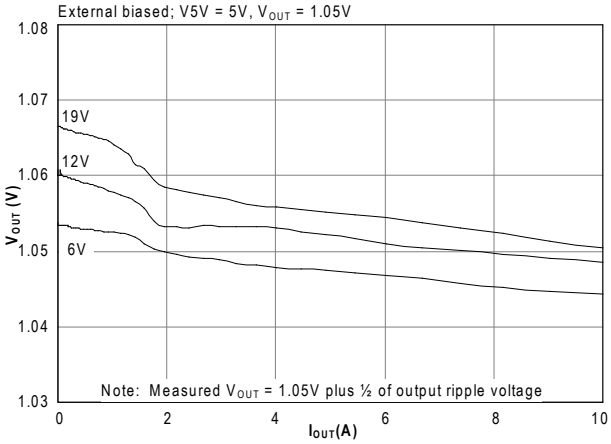
Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit on page 7 (SC417/SC427).

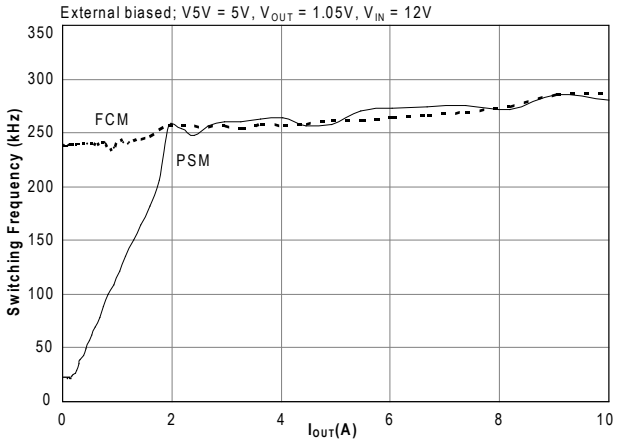
SC417 Load Regulation —FCM



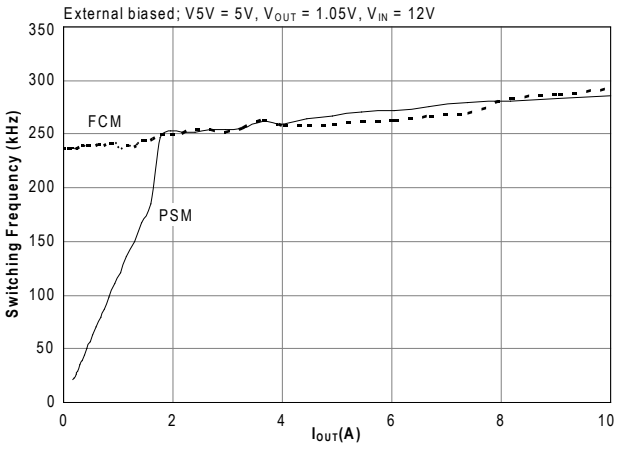
SC427 Load Regulation —FCM



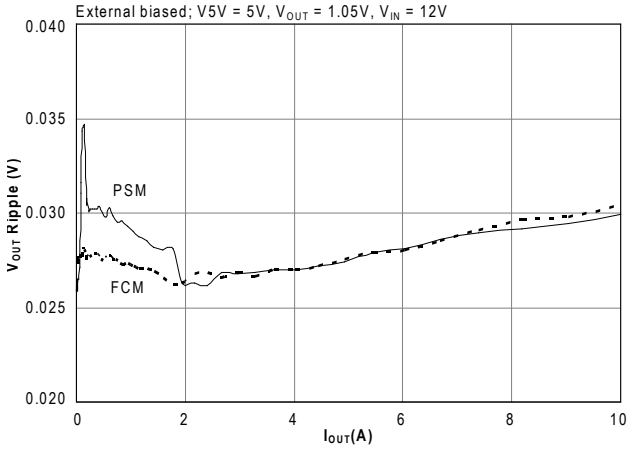
SC417 Switching Freq. — FCM vs. PSAVE Mode



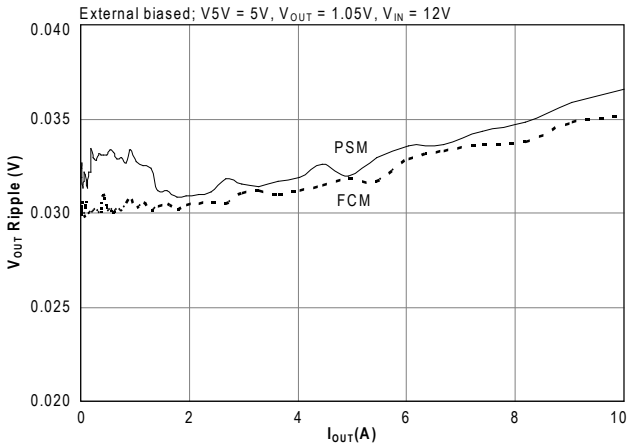
SC427 Switching Freq. — FCM vs. PSAVE Mode



SC417 V_{OUT} Ripple —FCM vs. PSAVE Mode



SC427 V_{OUT} Ripple —FCM vs. PSAVE Mode

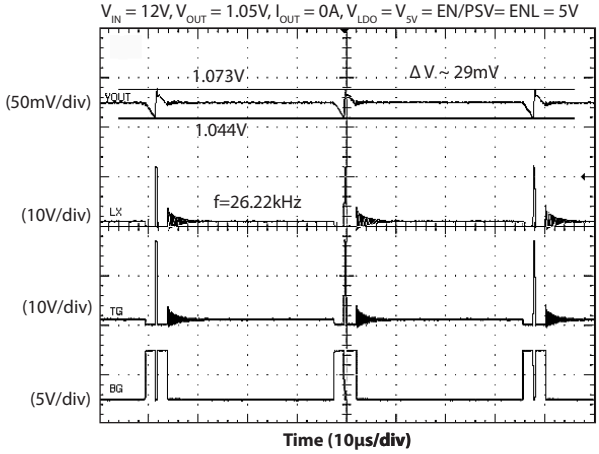


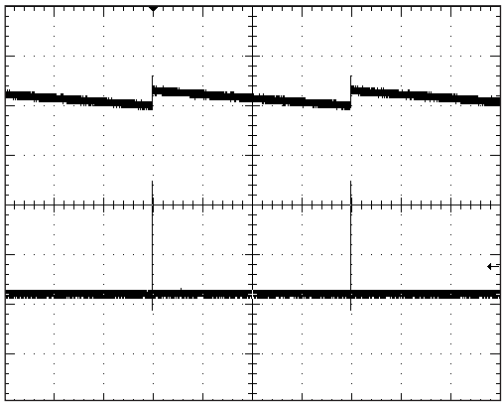
Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit on page 7 (SC417/SC427).

Ultrasonic Powersave Mode — No Load (SC417)

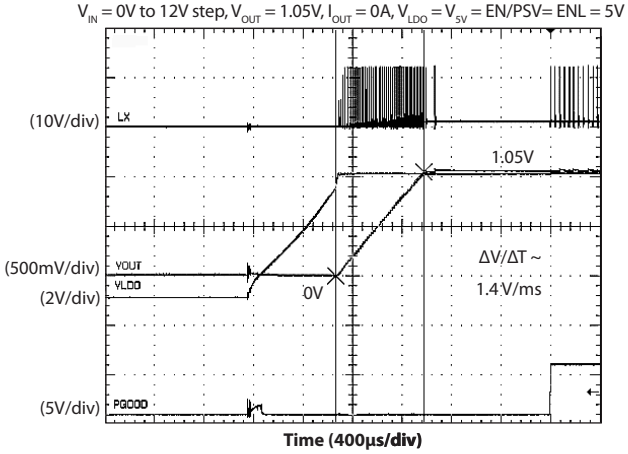
V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V





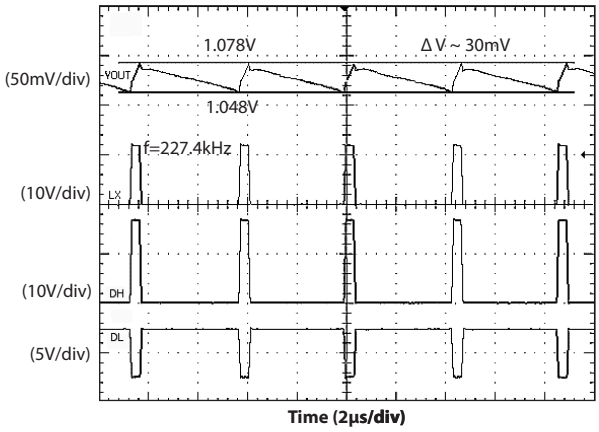
Self-Biased Start-Up — Power Good True

V_{IN} = 0V to 12V step, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



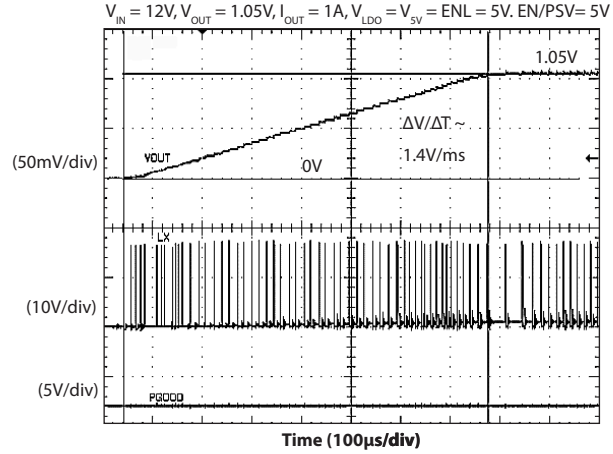
Forced Continuous Mode — No Load

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = ENL = 5V, EN/PSV= float



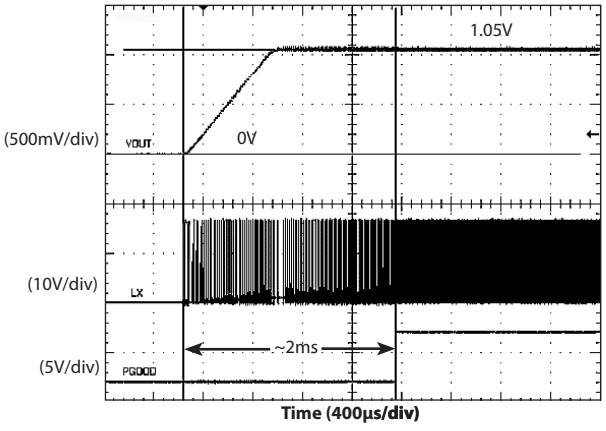
Enabled Loaded Output — Full Scale

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 1A, V_{LDO} = V_{5V} = ENL = 5V. EN/PSV= 5V



Enabled Loaded Output — Power Good True

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 1A, V_{LDO} = V_{5V} = ENL = 5V. EN/PSV= 5V

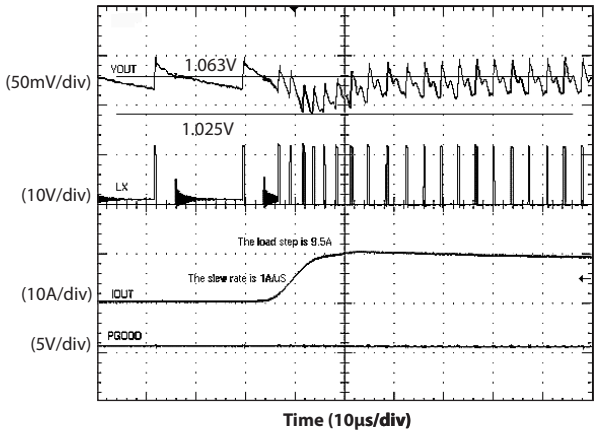


Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit on page 7 (SC417/SC427).

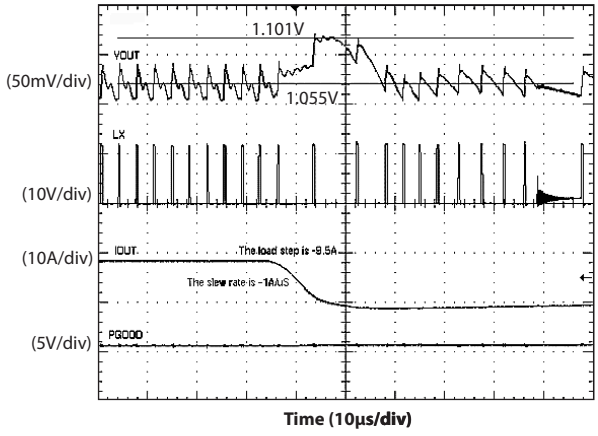
Transient Response — Load Rising (SC417)

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A to 10A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



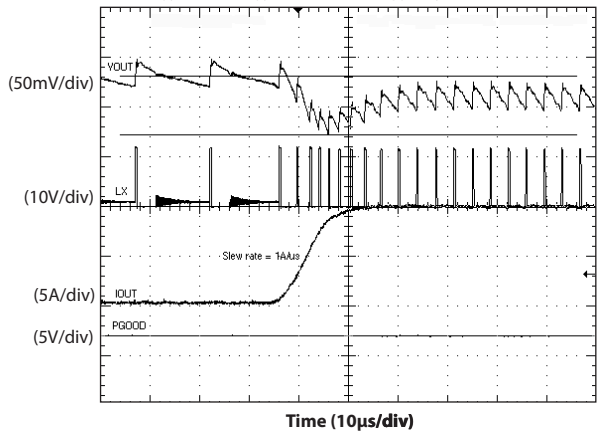
Transient Response — Load Falling (SC417)

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 10A to 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



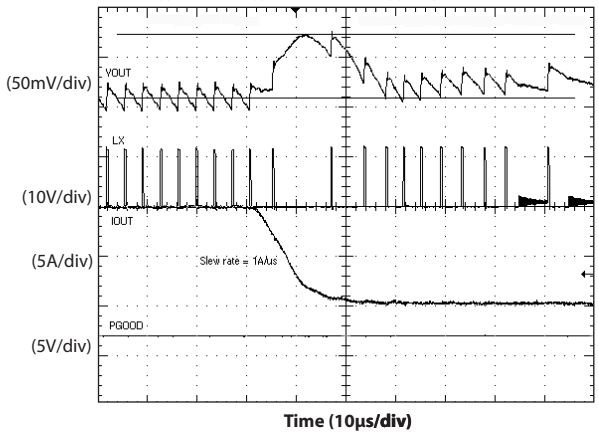
Transient Response — Load Rising (SC427)

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A to 10A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



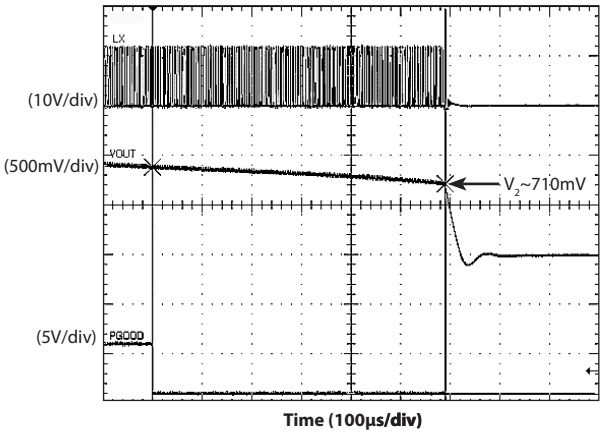
Transient Response — Load Falling (SC427)

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 10A to 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



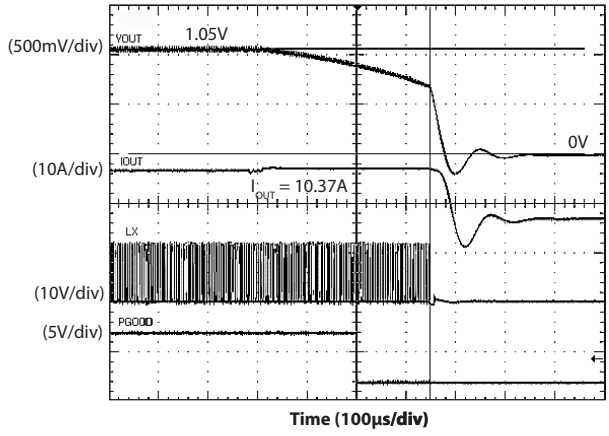
Output Under-voltage Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = ENL = 5V, floating EN/PSV



Output Over-current Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.05V, V_{LDO} = V_{5V} = ENL = 5V, EN/PSV= floating; I_{OUT} ramped to trip point

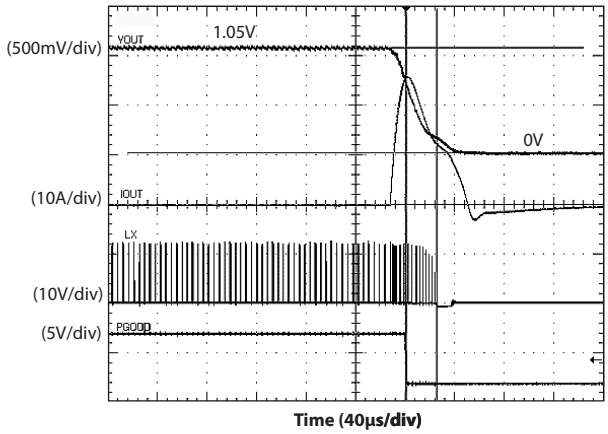


Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit on page 7 (SC417/SC427).

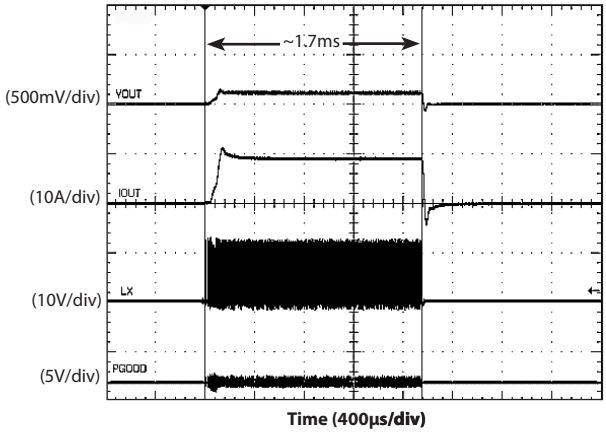
Shorted Output Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Shorted Output Response — Power-UP Operation

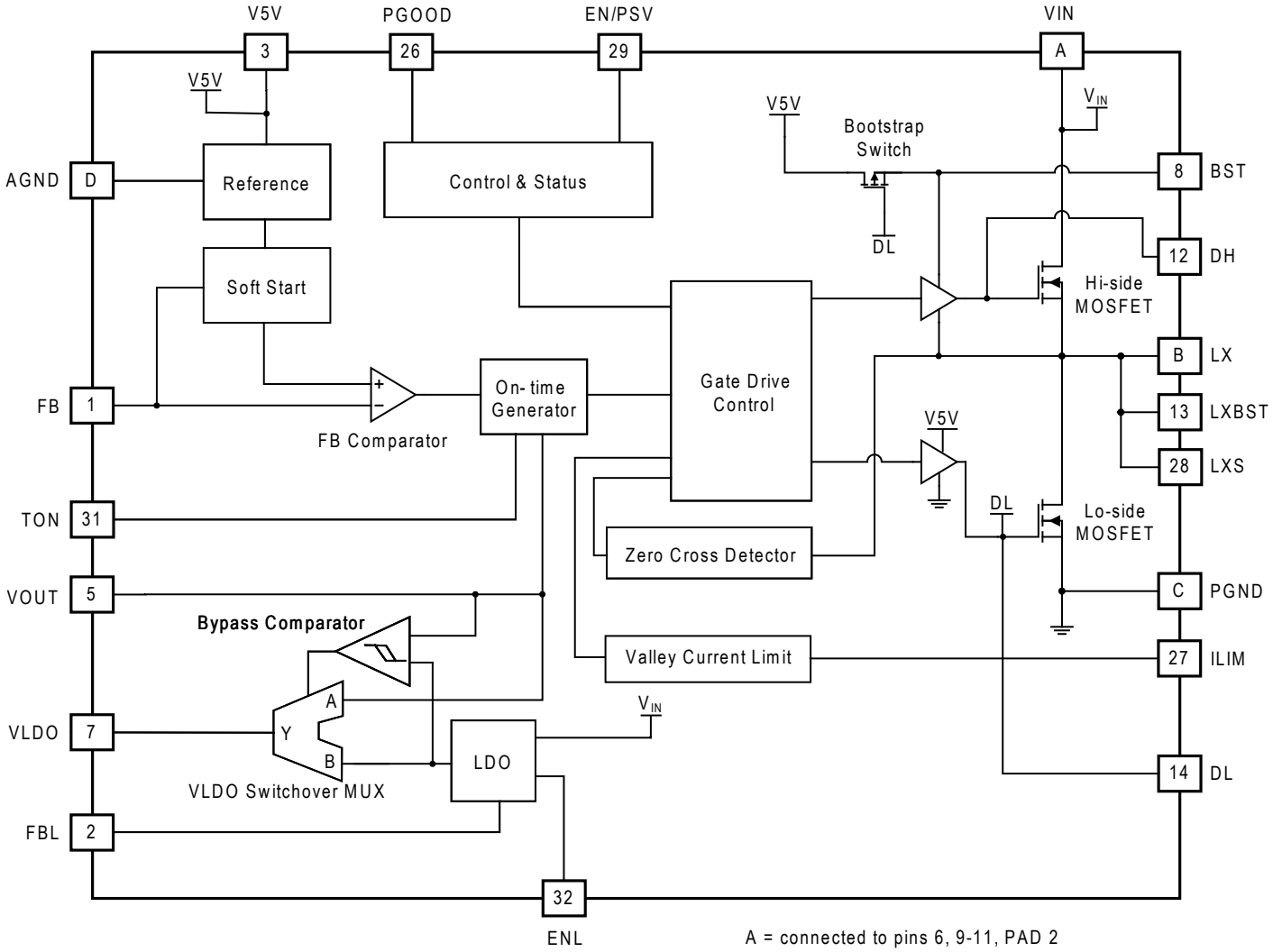
V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator used to program the output voltage — connect to an external resistor divider from VOUT to AGND.
2	FBL	Feedback input for the LDO — connect to an external resistor divider from VLDO to AGND — used to program the LDO output.
3	V5V	5V power input for internal analog circuits and gate drives — connect to external 5V supply or configure the LDO for 5V and connect to VLDO.
4, 30, PAD 1	AGND	Analog ground
5	VOUT	Switcher output voltage sense pin — also the input to the internal switch-over between VOUT and VLDO. The voltage at this pin must be less than or equal to the voltage at the V5V pin.
6, 9-11, PAD 2	VIN	Input supply voltage
7	VLDO	LDO output — The voltage at this pin must be less than or equal to the voltage at the V5V pin.
8	BST	Bootstrap pin — connect a capacitor of at least 100nF from BST to LX to develop the floating supply for the high-side gate drive.
12	DH	High-side gate drive — do not connect this pin
13	LXBST	LX Boost — connect to the BST capacitor.
23-25, PAD 3	LX	Switching (phase) node
14	DL	Low-side gate drive — do not connect this pin
15-22	PGND	Power ground
26	PGOOD	Open-drain power good indicator — high impedance indicates power is good. An external pull-up resistor is required.
27	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LX.
28	LXS	LX sense — connects to R_{ILIM}.
29	EN/PSV	Enable/power-save input for the switching regulator — connect to AGND to disable the switching regulator. Float to operate in forced continuous mode (power-save disabled). SC417 — connect to V5V to operate with ultra-sonic power-save mode enabled. SC427 — connect to V5V to operate with power-save mode enabled with no minimum frequency.
31	TON	On-time programming input — set the on-time by connecting through a resistor to AGND
32	ENL	Enable input for the LDO — connect ENL to AGND to disable the LDO. Drive with logic to +3V for logic control, or program the VIN UVLO with a resistor divider between VIN, ENL, and AGND.

Block Diagram



A = connected to pins 6, 9-11, PAD 2
B = connected to pins 23-25, PAD 3
C = connected to pins 15-22
D = connect to pins 4, 30, PAD 1

Applications Information

Synchronous Buck Converter

The SC417/SC427 is a step down synchronous DC-DC buck converter with integrated power MOSFETs and a programmable LDO. The device is capable of 10A operation at very high efficiency. A space saving 5x5 (mm) 32-pin package is used. The programmable operating frequency range of 200kHz to 1MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response which permits the use of smaller output capacitors.

In addition to the following information, the user can click on the applicable link to go to the SC417 online C-SIM design and simulation tool or to go to the SC427 online C-SIM design and simulation tool, which will lead the user through the design process.

Input Voltage Requirements

The SC417/SC427 requires two input supplies for normal operation: VIN and V5V. VIN operates over the wide range from 3V to 28V. V5V requires a 5V supply input that can be an external source or the internal LDO configured to supply 5V from VIN.

Power Up Sequence

When the SC417/SC427 uses an external power source at the V5V pin, the switching regulator initiates the start-up process when VIN, V5V, and EN/PSV are above their respective thresholds. When EN/PSV is at a logic high, V5V needs to be applied after VIN rises. To start using the EN/PSV pin when both V5V and VIN are above their respective thresholds, apply EN/PSV to enable the start-up process. For SC417/SC427 in self-biased mode, refer to the LDO section for a full description.

Shutdown

The SC417/SC427 can be shutdown by pulling either V5V or EN/PSV below its threshold. When V5V is active and EN/PSV at low logic, the output voltage discharges through an internal FET.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC417/SC427 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

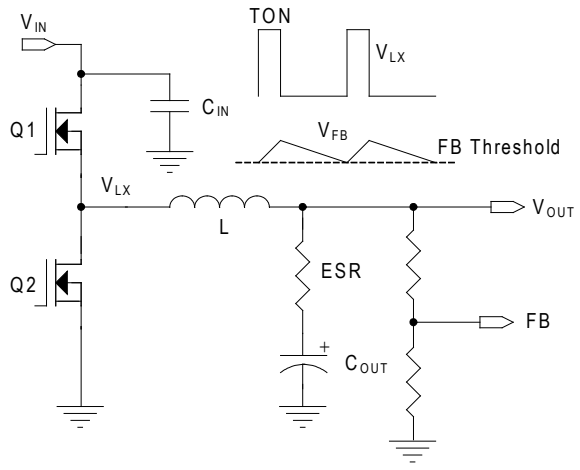


Figure 1 — PWM Control Method, V_{OUT} Ripple

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

One-Shot Timer and Operating Frequency

The one-shot timer operates as shown in Figure 2. The FB Comparator output goes high when V_{FB} is less than the

Applications Information (continued)

internal 500mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

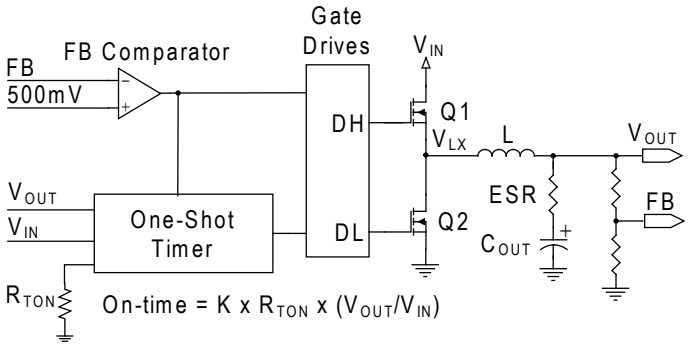


Figure 2 — On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC417/SC427 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{15\mu A}$$

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin (see Figure 3) to the internal 500mV reference voltage, see the Detailed Application Circuit.

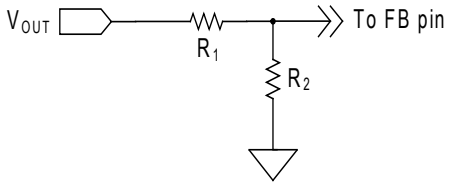


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

When a large capacitor is placed in parallel with R1 (C_{TOP}) V_{OUT} is shown by the following equation.

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

The switcher output voltage can be programmed higher than 5V. The VOUT pin is not allowed to connect directly to the switcher output due to its the maximum voltage rating. An additional resistor divider network is required to connect from the switcher output to the VOUT pin. When SC417/SC427 operates in self-biased mode, the minimum difference between the voltages for the VOUT and the VLDO pins should be ±500mV to avoid unwanted switchover function due to resistor divider voltage drop. For example, the voltage at the VOUT pin can be 4V if VLDO is set for 5V. When the SC417/SC427 operates from an external power source and the LDO is disabled, the voltage at the VOUT pin can be as high as shown in Recommended Operating Conditions. R_{TON} is calculated according to the voltage at the VOUT pin not the voltage of the switcher output.

Enable and Power-save Input

The EN/PSV input is used to enable or disable the switching regulator. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off,

Applications Information (continued)

the output of the switching regulator soft-discharges the output into a 15Ω internal resistor via the V_{OUT} pin. When EN/PSV is allowed to float, the pin voltage will float to 33% of the voltage at V5V. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode.

When EN/PSV is high (above 44% of the voltage at V5V) for SC417, the switching regulator turns on with ultra-sonic power-save enabled. The SC417 ultra-sonic power-save operation maintains a minimum switching frequency of 25kHz, for applications with stringent audio requirements.

When EN/PSV is high (above 44% of the voltage at V5V) for SC427, the switching regulator turns on with power-save enabled. The SC427 power-save operation is designed to maximize efficiency at light loads with no minimum frequency limits. This makes the SC427 an excellent choice for portable and battery-operated systems.

Forced Continuous Mode Operation

The SC417/SC427 operates the switcher in Forced Continuous Mode (FCM) by floating the EN/PSV pin (see Figure 4). In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs.

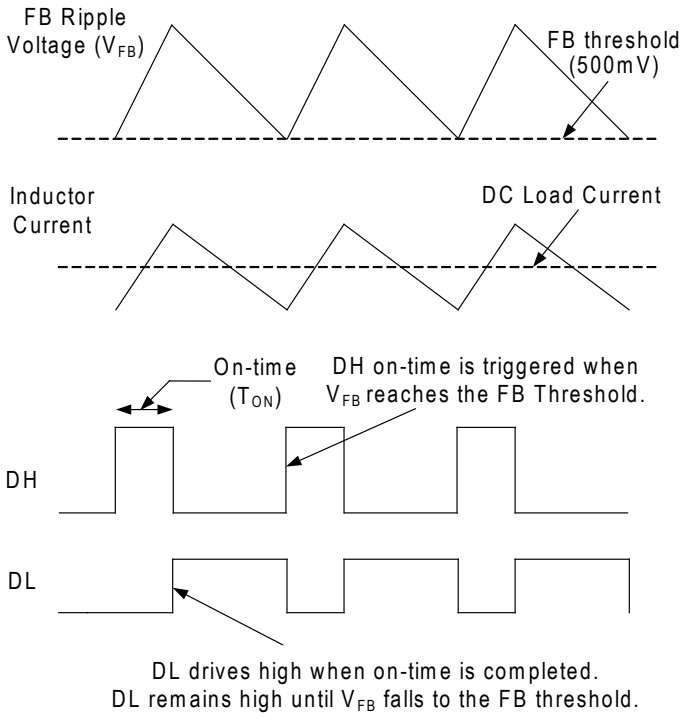


Figure 4 — Forced Continuous Mode Operation

Ultra-sonic Power-save Operation (SC417)

The SC417 provides ultra-sonic power-save operation at light loads, with the minimum operating frequency fixed at 25kHz. This is accomplished using an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds 40µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 500mV threshold, the next DH on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

Because the on-times are forced to occur at intervals no greater than 40µs, the frequency will not fall below ~25kHz. Figure 5 shows ultra-sonic power-save operation.

Applications Information (continued)

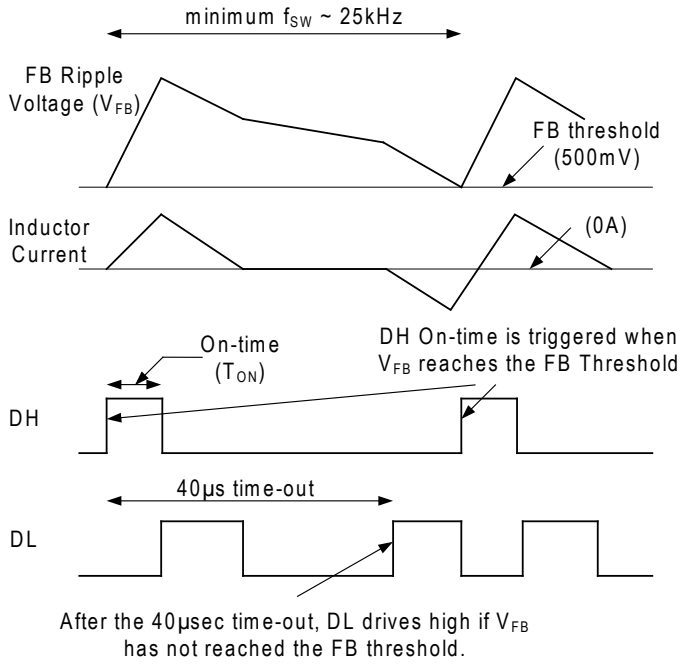


Figure 5 — Ultrasonic Power-save Operation

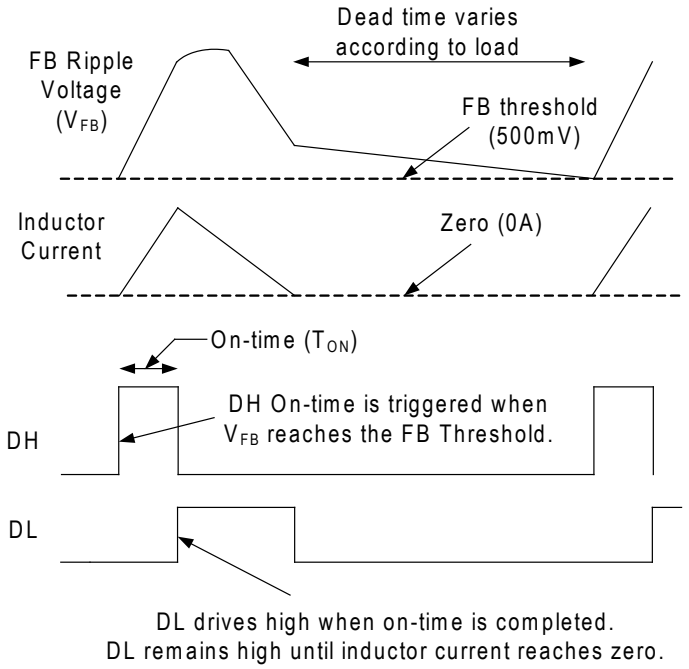


Figure 6 — Power-save Operation

Power-save Mode Operation (SC427)

The SC427 provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 500mV threshold. Because the MOSFETs are off, the load is supplied by the output capacitor. If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode. Figure 6 shows power-save operation at light loads.

Smart Power-save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutdown. Smart power-save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 550mV), the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 500mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 7 shows typical waveforms for the Smart Power-save feature.

SmartDrive™

For each DH pulse the DH driver initially turns on the high-side MOSFET at a lower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.5V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching while maintaining high efficiency and also avoids the need for snubbers or series resistors in the gate drive.

Applications Information (continued)

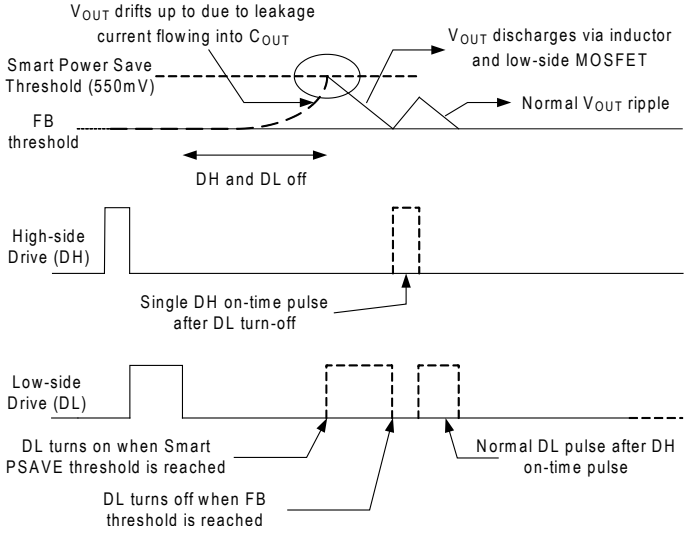


Figure 7 — Smart Power-save

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the RDS_{ON} of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the ILIM pin to the LX pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~10µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the RDS_{ON}. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by ILIM in Figure 8.

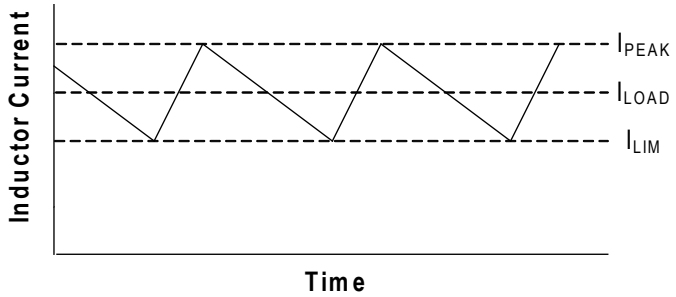


Figure 8 — Valley Current Limit

Setting the valley current limit to 10A results in a peak inductor current of 10A plus peak ripple current. In this situation, the average (load) current through the inductor is 10A plus one-half the peak-to-peak ripple current.

The internal 10µA current source is temperature compensated at 4100ppm in order to provide tracking with the RDS_{ON}.

The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 735 \times I_{LIM}$$

When selecting a value for R_{ILIM} be sure not to exceed the absolute maximum voltage value for the ILIM pin. Note that because the low-side MOSFET with low RDS_{ON} is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. R_{ILIM} should be connected directly to LXS (pin 28).

Soft-Start of PWM Regulator

Soft-start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB Comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 500mV in ~1.2mV increments, using an internal ~500kHz oscillator. When the ramp voltage reaches 500mV, the ramp is ignored and the FB comparator switches over to a fixed 500mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft-start profile for a wide range of applications. Typical soft-start ramp time is 850µs.

Pre-Bias Startup

SC417/427 can start up into a pre-biased output voltage. The start up time is approximately 850µs from enable to regulation. The output voltage starts to ramp up when the internal ramp meets the pre-charged FB voltage level. Pre-bias startup is achieved by turning off the lower gate when the inductor current falls below zero. This method prevents output voltage discharge.

Applications Information (continued)

Power Good Output

The power good (PGOOD) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns above -8% of nominal. PGOOD is held low during start-up and will not be allowed to transition high until soft-start is completed (when V_{FB} reaches 500mV) and typically 2ms has passed.

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold (600mV). PGOOD also pulls low if the EN/PSV pin is low when V5V is present.

Output Over-Voltage Protection

Over-voltage protection becomes active as soon as the device is enabled. The threshold is set at 500mV + 20% (600mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or V5V is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage (falls to 375mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs. The controller stays off until EN/PSV is toggled or V5V is cycled.

V5V UVLO, and POR

Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until V5V rises above 3.9V. An internal Power-On Reset (POR) occurs when V5V exceeds 3.9V, which resets the fault latch and soft-start counter to prepare for soft-start. The SC417/SC427 then begins a soft-start cycle. The PWM will shut off if V5V falls below 3.6V.

LDO Regulator

The LDO output is programmable from 0.75V to 5.25V using external resistors. The feedback pin (FBL) for the LDO is regulated to 750mV. There is also an enable pin (ENL) for the LDO that provides independent control. The LDO voltage can also be used to provide the bias voltage for the switching regulator. When a separate source is used as the bias supply, the LDO can be programmed to provide a different voltage (see Figure 9).

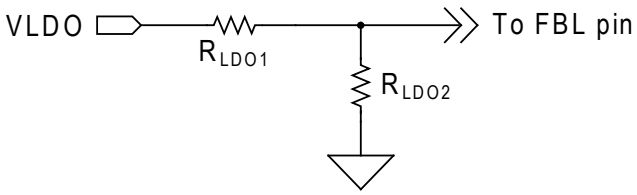


Figure 9 — LDO Start-Up

The LDO output voltage is set by the following equation.

$$VLDO = 750mV \times \left(1 + \frac{R_{LDO1}}{R_{LDO2}}\right)$$

A minimum capacitance of 1µF referenced to AGND is normally required at the output of the LDO for stability. If the LDO is providing bias power to the device, then a minimum 0.1µF capacitor referenced to AGND is required along with a minimum 1.0µF capacitor referenced to PGND to filter the gate drive pulses. Refer to the layout guidelines section.

LDO ENL Functions

The ENL input is used to enable/disable the internal LDO. When ENL is a logic low, the LDO is off. When ENL is a high but below the VIN UVLO threshold (2.6V typical), then the LDO is on and the switcher is off. When ENL is above the V_{IN} UVLO threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV pin is not grounded. The table below summarizes the function of ENL and EN/PSV pins.

EN/PSV	ENL	LDO	Switcher
Disabled	Low, < 0.4V	OFF	OFF
Enabled	Low, < 0.4V	OFF	ON
Disabled	1.0V < High < 2.6V	ON	OFF
Enabled	1.0V < High < 2.6V	ON	OFF
Disabled	High, > 2.6V	ON	OFF
Enabled	High, > 2.6V	ON	ON

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. When SC417/SC427 is self-biased from the LDO and runs from the V_{IN} power source only, the VIN UVLO feature can be used to prevent false UV faults for the PWM output by programming with a resistor divider at the VIN, ENL and AGND pins. When SC417/SC427 has an exter-

Applications Information (continued)

nal bias voltage at V5V and the ENL pin is used to program the VIN UVLO feature, the voltage at FBL needs to be higher than 750mV to force the LDO off.

Timing is important when driving ENL with logic and not implementing V_{IN} UVLO. The ENL pin must transition from high to low within 2 switching cycles to avoid the PWM output turning off. If ENL goes below the VIN UVLO threshold and stays above 1V, then the switcher will turn off but the LDO will remain on.

Additional protection logic is included in the SC417/SC427 to allow for maximum flexibility of the IC and controlled starting in self-biased mode. In self-biased mode where the LDO and PWM are started at the same time, the PWM output will not start until the LDO reaches 90% of it's final value. This prevents overloading the current limited LDO output during LDO start up. When using the LDO as an independent output, it is desirable to be able to turn the LDO on and off independent of the PWM output. This is accomplished by checking the PWM PGOOD output during start-up. If PGOOD is high when the LDO turns on then the two outputs are assumed to be independent and the LDO start-up will not effect the PWM. If the PGOOD output is low then the part is assumed to be in self-biased mode and the PWM turn-on is delayed until the LDO start-up is 90% complete.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. VLDO output
3. V_{IN} input voltage

When the ENL pin is high and V_{IN} is above the UVLO point, the LDO will begin start-up. During the initial phase, when the LDO output voltage is near zero, the LDO initiates a current-limited start-up (typically 85mA) to charge the output capacitor. When V_{LDO} has reached 90% of the final value (as sensed at the FBL pin), the LDO current limit is increased to ~200mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator (see Figure 10).

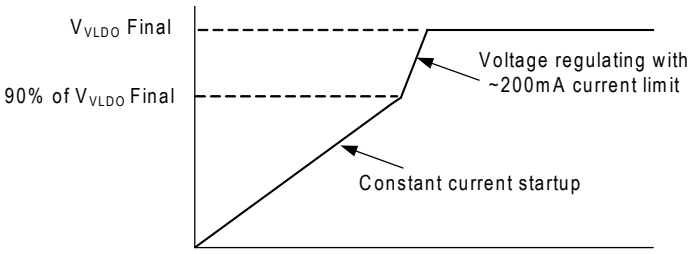


Figure 10 — LDO Start-Up

LDO Switch-Over Operation

The SC417/SC427 includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient DC-DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the VLDO pin directly to the VOUT pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SC417/SC427, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over logic waits for 32 switching cycles before it starts the switch-over. There are two methods that determine the switch-over of V_{LDO} to V_{OUT}.

In the first method, the LDO is already in regulation and the DC-DC converter is later enabled. As soon as the PGOOD output goes high, the 32 cycles are started. The voltages at the VLDO and VOUT pins are then compared; if the two voltages are within ±300mV of each other, the VLDO pin connects to the VOUT pin using an internal switch, and the LDO is turned off.

In the second method, the DC-DC converter is already running and the LDO is enabled. In this case the 32 cycles are started as soon as the LDO reaches 90% of its final value. At this time, the VLDO and VOUT pins are compared, and if within ±300mV the switch-over occurs and the LDO is turned off.

Switch-over Limitations on VOUT and VLDO

Because the internal switch-over circuit always compares the VOUT and VLDO pins at start-up, there are limitations on permissible combinations of these pins. Consider the case where V_{OUT} is programmed to 3.0V and V_{LDO} is pro-

Applications Information (continued)

grammed to 3.3V. After start-up, the device would connect VOUT to VLDO and disable the LDO, since the two voltages are within the ±300mV switch-over window. To avoid unwanted switch-over, the minimum difference between the voltages for V_{OUT} and V_{LDO} should be ±500mV.

It is not recommended to use the switch-over feature for an output voltage less than 3V since this does not provide sufficient voltage for the gate-source drive to the internal p-channel switch-over MOSFET.

Switch-over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in Figure 11.

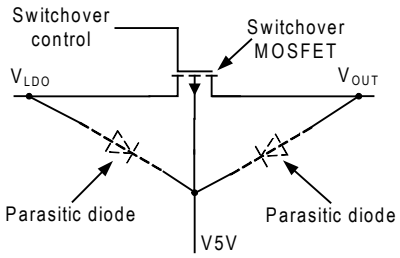


Figure 11— Switch-over MOSFET Parasitic Diodes

There are some important design rules that must be followed to prevent forward bias of these diodes. The following two conditions need to be satisfied in order for the parasitic diodes to stay off.

- $V5V \geq V_{LDO}$
- $V5V \geq V_{OUT}$

If either V_{LDO} or V_{OUT} is higher than V5V, then the respective diode will turn on and the SC417/SC427 operating current will flow through this diode. This has the potential of damaging the device.

Using the On-chip LDO to Bias the SC417/SC427

The following steps must be followed when using the on-chip LDO to bias the device.

- Connect V5V to VLDO before enabling the LDO.
- The LDO has an initial current limit of 85mA at start-up, therefore, do not connect any external load to VLDO during start-up.
- When VLDO reaches 90% of its final value, the LDO current limit increases to 200mA. At this time the LDO may be used to supply the required bias current to the device.

Attempting to operate in self-powered mode in any other configuration can cause unpredictable results and may damage the device.

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- $V_{IN} = 12V \pm 10\%$
- $V_{OUT} = 1.05V \pm 4\%$
- $f_{SW} = 250kHz$
- Load = 10A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

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Applications Information (continued)

The desired switching frequency is 250kHz which results from using components selected for optimum size and cost.

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 318 ns at 13.2V_{IN}, 1.05V_{OUT}, 250kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 154.9kΩ, use R_{TON} = 154kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then Power-save operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50% of the maximum load current. Therefore ripple current will be 50% x 10A or 5A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2 - 1.05) \times 318ns}{5A} = 0.77\mu H$$

A slightly larger value of 0.88µH is selected. This will decrease the maximum I_{RIPPLE} to 4.4A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 384ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(10.8 - 1.05) \times 384ns}{088\mu H} = 4.25A$$

Output Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is that the output voltage regulation be ±4% under static conditions. The internal 500mV reference tolerance is 1%. Allowing 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple.

Applications Information (continued)

Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 42mV for a 1.05V output.

The maximum ripple current of 4.4A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{42mV}{4.4A}$$

$$ESR_{MAX} = 9.5\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (100mV rise upon load release), and a 10A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{0.88\mu H\left(10 + \frac{1}{2} \times 4.4\right)^2}{(1.15)^2 - (1.05)^2}$$

$$COUT_{MIN} = 595\mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 500mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt.

Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 10 + 1/2 \times 4.4 = 12.2A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 10A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2.5A}{\mu s}$$

This would cause the output current to move from 10A to 0A in 4µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 12.2 \times \frac{0.88\mu H \times \frac{12.2}{1.05} - \frac{10}{2.5} \times 1\mu s}{2(1.15 - 1.05)}$$

$$C_{OUT} = 379\ \mu F$$

Note that C_{OUT} is much smaller in this example, 379µF compared to 595µF based on a worst-case load release. To meet the two design criteria of minimum 379µF and maximum 9mΩ ESR, select two capacitors rated at 220µF and 15mΩ ESR.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Applications Information (continued)

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 13. This capacitor should be left unpopulated until it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

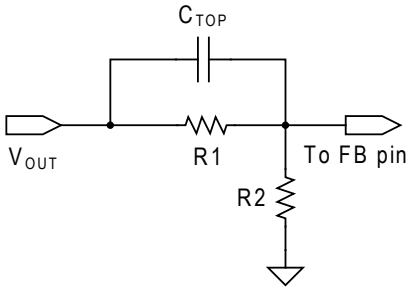


Figure 13 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is a decrease in load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Using Ceramic Output Capacitors

For applications using ceramic output capacitors, the ESR is normally too small to meet the above ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in Figure 14. This network creates a ramp voltage across C_L, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitively coupled into the FB pin via capacitor C_C.

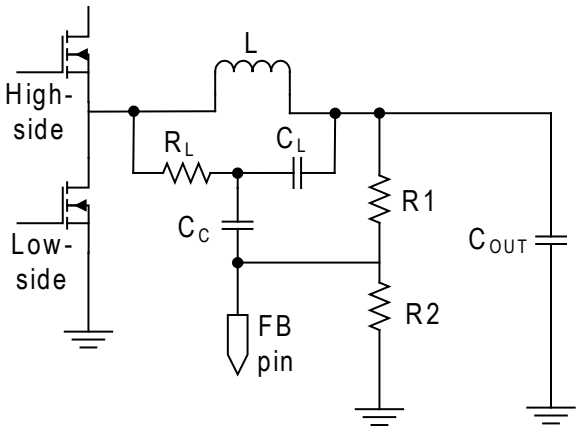


Figure 14 — Virtual ESR Ramp Current

Applications Information (continued)

The component values used in this circuit are calculated using the following procedure.

Select C_L (100nF) and R_L to provide a 25mV ripple across C_L (V_{CL}).

$$R_L = \frac{V_{IN} - V_{OUT}}{I_{CL}}$$

where

$$I_{CL} = \frac{C_L \times \Delta V_{CL}}{T_{ON}}$$

and

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Next choose a value for C_C so that

$$C_C = \frac{T_{ON}}{R_{EQ}}$$

where

$$R_{EQ} = \frac{R_1 \times R_2}{R_1 + R_2}$$

The resistor values (R_1 and R_2) in the voltage divider circuit set the V_{OUT} for the switcher.

Choosing Input Capacitors

Input capacitors bank is used to provide AC current to the power stage when the high side FET turns on and especially during the output current step up. The ripple current rating of the input capacitors must meet or exceed I_{RMS} ripple caused by the switching currents. The ripple current generated is calculated using the following equation.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = 10A \times \frac{\sqrt{1.05V \times (12V - 1.05V)}}{12V} = 2.83A$$

Because of their low ESR and ESL, ceramic capacitors are typically used. High quality dielectric capacitors should be used (for example X5R or X7R). The effective capacitance of ceramic capacitors varies under DC bias and temperature. Another factor of selecting the input capacitors is its voltage rating which needs to be higher than the maximum input voltage because the ringing on the LX node. While a single capacitor is sufficient to handle the ripple current, additional ceramic capacitors or bulk capacitors may be needed to provide local energy storage and a low impedance input source to account for any PCB or input connector impedances.

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 250ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 500mV, 1%.

The on-time pulse from the SC417/SC427 in the design example is calculated to give a pseudo-fixed frequency of 250kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

Applications Information (continued)

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors may result in up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

Applications Information (continued)

PCB Layout Guidelines

The optimum layout for the SC417/SC427 is shown in Figure 15. This layout shows an integrated FET buck regulator with a maximum current of 10A. The total PCB area is approximately 20 x 25 mm.

Critical Layout Guidelines

The following critical layout guidelines must be followed to ensure proper performance of the device.

- IC Decoupling capacitors
- PGND plane
- AGND island
- FB, VOUT, and other analog control signals
- BST, ILIM, and LX
- CIN and COUT placement and Current Loops

IC Decoupling Capacitors

- A 0.1 µF capacitor must be located as close as possible to the IC and directly connected to pins 3 (V5V) and 4 (AGND).
- All other decoupling capacitors must be located as close as possible to the IC.

PGND Plane

- PGND requires its own copper plane with no other signal traces routed on it.
- Copper planes, multiple vias and wide traces are needed to connect PGND to input capacitors, output capacitors, and the PGND pins on the IC.
- The PGND copper area between the input capacitors, output capacitors and PGND pins must be as tight and compact as possible to reduce the area of the PCB that is exposed to noise due to current flow on this node.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

AGND Island

- AGND should have its own island of copper with no other signal traces routed on this layer that connects the AGND pins and pad of the IC to the analog control components.
- All of the components for the analog control circuitry should be located so that the connections

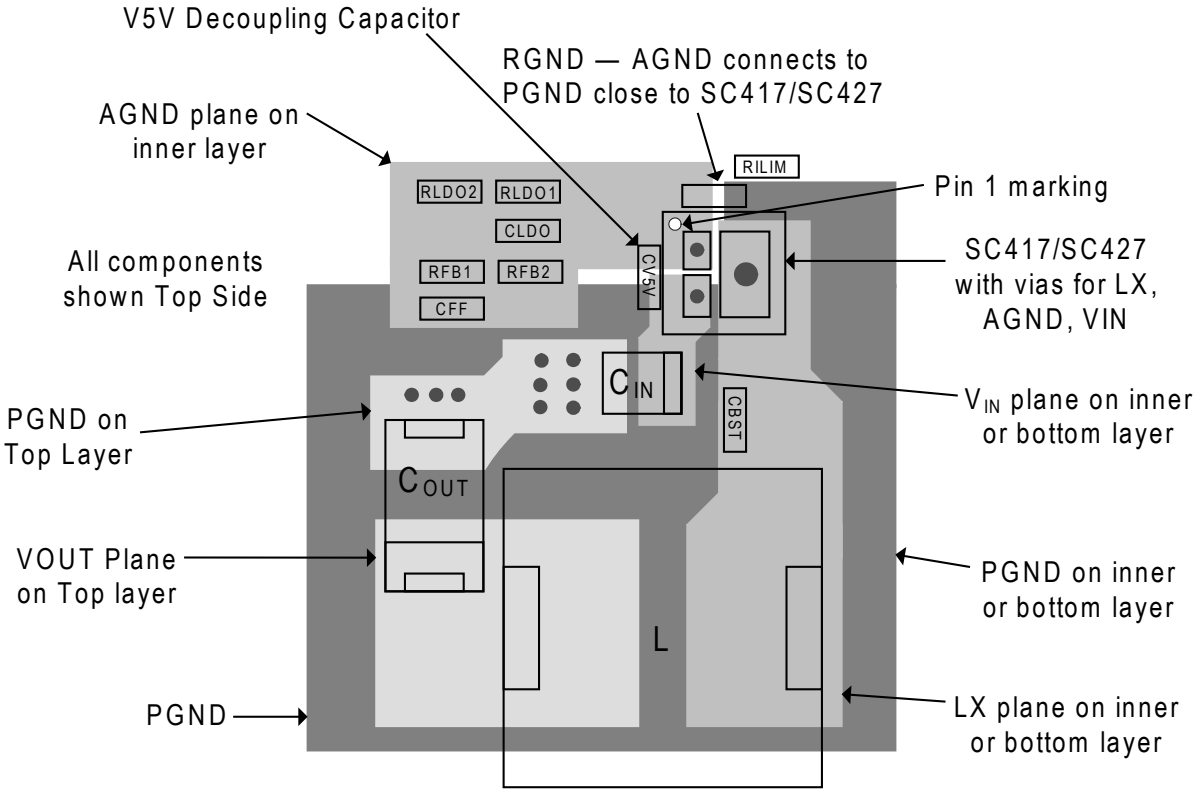


Figure 15 — PCB Layout

Applications Information (continued)

to AGND are done by wide copper traces or vias down to AGND.

- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

FB, VOUT, and Other Analog Control Signals

- The connection from the V_{OUT} power to the analog control circuitry must be routed from the output capacitors and located on a quiet layer.
- The traces between Vout and the analog control circuitry (VOUT, and FB pins) must be short and routed away from noise sources, such as BST, LX, VIN, and PGND between the input capacitors, output capacitors, and the IC.
- ILIM and TON nodes must be as short as possible to ensure the best accuracy in current limit and on time.
- R_{ILIM} should be close to the IC and connected to LX with a Kelvin trace to pin 28 on the IC. All of the LX pins are connected to the LX PAD on the IC, which should be a sufficient connection and will prevent the need to connect the resistor further into the LX plane.
- The feedback components for the switcher and the LDO need to be as close to the FB and FBL pins of the IC as possible to reduce the possibility of noise corrupting these analog signals.

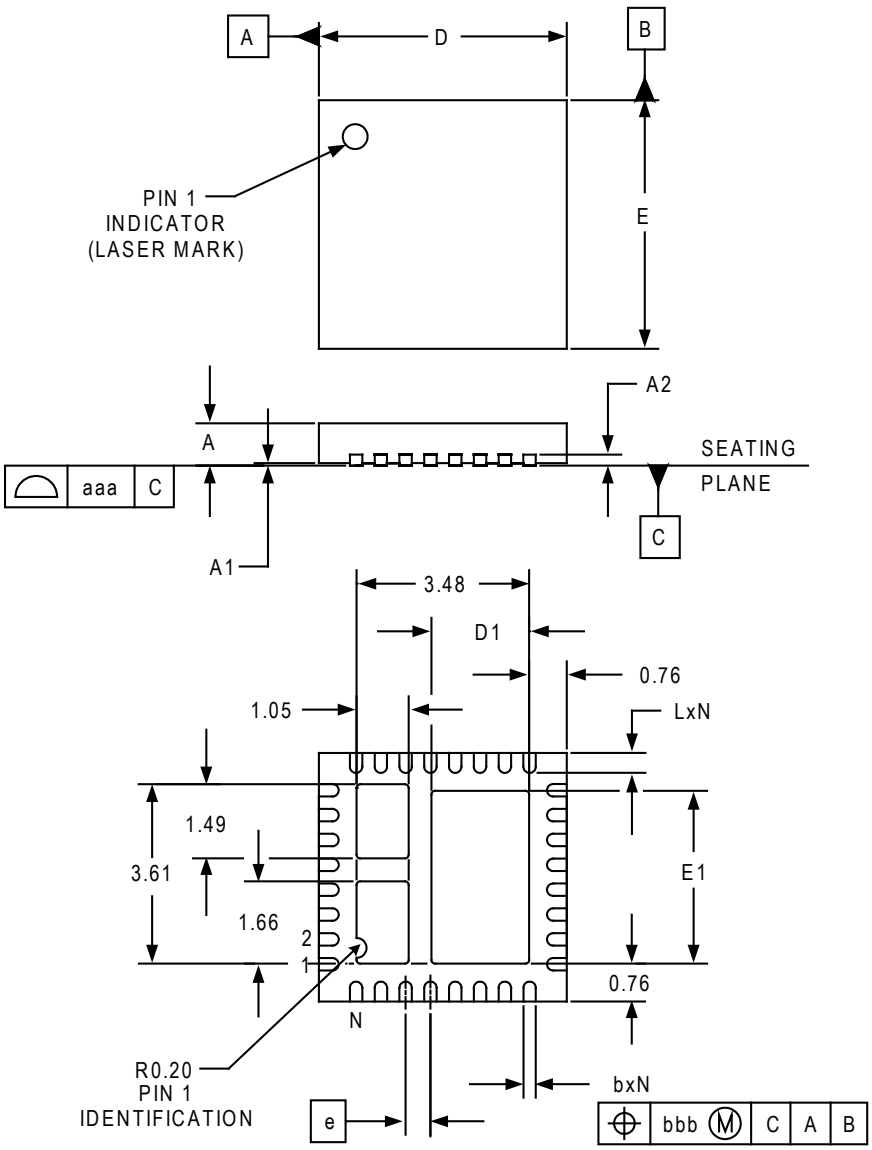
BST, ILIM and LX

- LX and BST are very noisy nodes and must be routed to minimized the PCB area that is exposed to these signals.
- The connections for the boost capacitor between the IC and LX must be short and directly connected to the LXBST (pin 13).
- The connections for the current limit resistor between the ILIM pin and LX must be as short as possible and directly connected to pin 28 (LXS).
- The LX node between the IC and the inductor should be wide enough to handle the inductor current and short enough to eliminate the possibility of LX noise corrupting other signals.
- Multiple vias should be used to provide a good connection to LX between the IC and the inductor.

Capacitors and Current Loops

- The current loops between the input capacitors, the IC, the inductor, and the output capacitors must be as close as possible to each other to reduce IR drop across the copper.
- All bypass and output capacitors must be connected as close as possible to the pin on the IC.

Outline Drawing — MLPQ-5x5-32



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.076	.078	.080	1.92	1.97	2.02
E	.193	.197	.201	4.90	5.00	5.10
E1	.135	.137	.139	3.43	3.48	3.53
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

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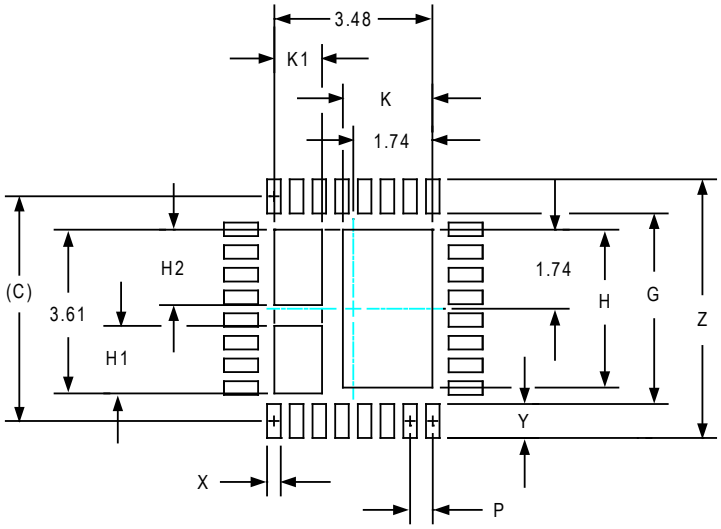
Land Pattern — MLPQ-5x5-32



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.195)	(4.95)
G	.165	4.20
H	.137	3.48
H1	.059	1.49
H2	.065	1.66
K	.078	1.97
K1	.041	1.05
P	.020	0.50
X	.012	0.30
Y	.030	0.75
Z	.224	5.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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