

**POWER MANAGEMENT****Description**

The SC2647 provides microprocessor core voltage regulation solution up to 4 paralleled PWM channels. The solution can also be configured as 2, 3, or 4-phase form. Multi-phase buck regulator utilizes the phase-shift timing control to allow interleaved switching of the power switches. This architecture minimizes the core voltage ripple and the input current ripple, which leads to optimized voltage regulator design for power density, transient responses, and the thermal performances.

To satisfy the highly dynamic nature of the modern microprocessors, the SC2647 adopts peak current mode control topology which ensures wide control loop bandwidth and fast transient responses. The current mode control provides intrinsic phase current matching. The maximum ripple frequency is greater than 1MHz.

One of the outstanding features of the SC2647 is its voltage regulation accuracy. Not only it provides better than 0.5% set point accuracy, but also the accuracy to fully complaint with the stringent load line slope specifications mandated by the modern microprocessors. Lossless output current sensing ensures the regulator output voltage is accurately positioned according to the load current condition, and an internal temperature compensation technology further enhances the performance of voltage accuracy.

The patented Combi-Sense™ topology is employed by SC2647. The MOSFET  $R_{ds(on)}$  and the output inductor winding resistance is used to generate the phase current information. The SC1211VX Combi-Sense™ MOSFET driver plus the SC2647 enables the complete solution.

The SC2647 is a multi-platform controller. It conforms to Intel VRM/VRD10.0, VRM9.X, and AMD K-8 (Opteron™) VID specifications. With very minor changes of the schematic and the layout, the SC2647 based solution can be ported from one platform to another. This greatly benefits the system manufactures for reductions of design cycle and minimize the inventory management.

The VID structure of the SC2647 supports VID-on-Fly applications for any platform. The cycle-by-cycle current limit plus the intelligent over current shut down provide the maximum versatility of the system without false tripping under all possible changes of VID and load conditions. The differential voltage feedback sense eliminates the error caused by high load current on the ground plane. External offset is easy to achieve for any platforms and the VID settings. The enable function is also provided to interface with the corresponding system signal for correct start up timing and shut down timing.

**(Multiple Patents Pending)**

**Features**

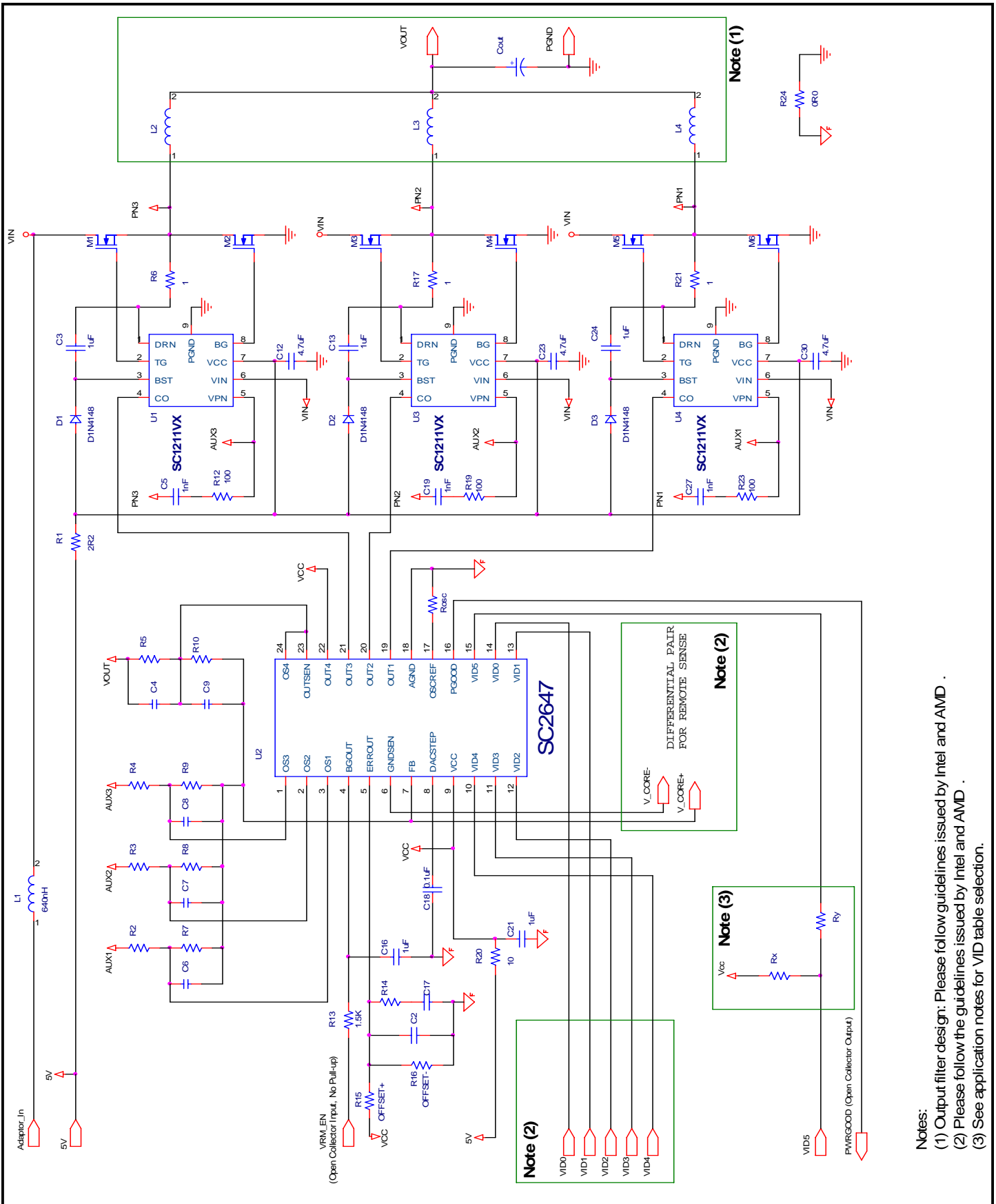
- ◆ VRD/VRM10.0, VRM9.X, and K-8 compliant
- ◆ Core Voltage Set Point Accuracy 0.5%
- ◆ Combi-Sense™ Current Mode Control
- ◆ Intrinsic Phase Current Matching
- ◆ Fast Transient Responses
- ◆ Active Droop with Temperature Compensation to Meet Load Line Slope
- ◆ Support VID-on-Fly with 5 or 6 bit VID
- ◆ Enable Function for Power Sequencing
- ◆ Cycle-by-Cycle Peak Current Limit
- ◆ Intelligent Over Current Shut Down
- ◆ Over Voltage Protection When Using Semtech Combi-Sense™ Driver/1211VX
- ◆ Under Voltage Protection Built in
- ◆ External programmable Soft-Start
- ◆ Externally programmable switching frequency.
- ◆ 2, 3, or 4-Phase Configurations
- ◆ 24-Pin SOIC or TSSOP Packages
- ◆ This device is fully WEEE and RoHS Compliant

**Applications**

- ◆ Voltage Regulator VRD/VRM10.0
- ◆ Voltage Regulator VRM9.X
- ◆ Voltage Regulator K-8
- ◆ High Current, Low Voltage Step Down DC/DC Converters

**POWER MANAGEMENT**

Typical Application Circuit



Notes:  
 (1) Output filter design: Please follow guidelines issued by Intel and AMD .  
 (2) Please follow the guidelines issued by Intel and AMD .  
 (3) See application notes for VID table selection.

**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	$V_{CC}$	20	V
Combi-Sense/Direct Output Voltage	OS1, OS2, OS3, OS4, OUTSEN	5	V
Ambient Temperature Range	$T_A$	0 to 105	°C
Junction Temperature Range	$T_J$	0 to 125	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	$T_{LEAD}$	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

**Electrical Characteristics**

Unless specified:  $V_{CC} = 5V$ , VID=1.30V (110110,VRD10) or 1.50V (101110,VRD10),  $F_{OSC} = 600kHz$ ,  $T_A = 27^\circ C$ . See Typical Application Circuit.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Chip_Supply</b>						
IC Supply Voltage	$V_{CC}$		4.7	5	7	V
IC Supply Current	$I_{CC}$			9.5		mA
UVLO Ramp Up				4.3		V
UVLO Hysteresis				300		mV
<b>Reference Section</b>						
Bandgap Output	$V_{BGOUT}$	$C_{BGOUT} = 4.7nF$		3		V
Source Current		BG=0V		270		$\mu A$
Sink Current		BG=4V		-500		$\mu A$
Supply Rejection		$V_{CC} = 4.7V \sim 7V$		0.5		mV/V
Temperature Stability		$0^\circ C < T_A < 85^\circ C$		0.5		%
VID Step		VRM9.X, K-8, LSB		25		mV
VID Step		VRD/VRM10, LSB		12.5		mV
Voltage Accuracy	$V_{OUT}$	VRD10 ; Internal offset=-20mV	-0.5		+0.5	%
		VRM9.x ; Internal offset=-20mV	-1		+1	%
		K-8 ; Internal offset=+25mV	-1		+1	%
<b>Oscillator Section</b>						
Oscillator Frequency		$R_{OSC} = 309Kohm$	540	600	660	kHz
Temperature Stability		$0^\circ C < T_A < 85^\circ C$		+/-5		%

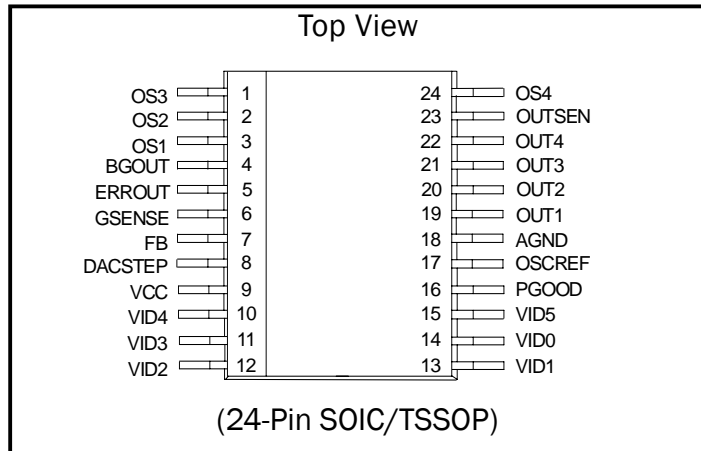
**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified:  $V_{CC} = 5V$ ,  $V_{ID} = 1.30V$  (110110,VRD10) or  $1.50V$  (101110,VRD10),  $F_{osc} = 600kHz$ ,  $T_A = 27^\circ C$ . See Typical Application Circuit.

Parameter	Test Conditions	Min	Typ	Max	Units
<b>Voltage Error Amplifier</b>					
Input Offset Voltage			+/-3		mV
Input Bias Current			25		nA
Open Loop Gain	$1V < V_{ERROUT} < 3.6V$		80		dB
Unity Gain Bandwidth	$C_{ERROUT} = 10pF$		10		MHz
Slew Rate			2		V/ $\mu$ S
Transconductance Gain			0.5		mA/V
<b>Current Sense Amplifiers</b>					
Input Offset Voltage			+/-3		mV
Input Bias Current			50		nA
Gain			9.5		V/V
CMRR	0 to 3V		80		dB
Input Common Mode Range		-0.3		3	V
Gain Match			2		%
Bandwidth			6		MHz
<b>Droop Amplifier</b>					
Gain			5.2		V/V
<b>VIDs</b>					
Logic Threshold	[VID0:4]	1.2		1.8	V
Pull-up Impedance	[VID0:4]		10		Kohm
VID5 Logic Threshold for VRD/VRM10	VID5	1.2		1.8	V
VID5 Clamping voltage			2.7		V
VID5 Selection Threshold for VRM9.X	VID5/Sink		49		$\mu$ A
VID5 Selection Threshold for K-8	VID5/Sink		205		$\mu$ A
<b>3-Phase Operation</b>					
Output 4 pull up Threshold		3.7	4.1		V
<b>Power Good</b>					
Threshold Rising	VID - Power Good Threshold		330		mV
Threshold Falling	VID - Power Good Threshold		560		mV
Output High Leakage	$P_{wrgood} = V_{CC}$		100		nA
Output Low Sink	$P_{wrgood} = 0.8V$	2			mA
<b>Current Limit Section</b>					
Max. Error Amp Voltage for Current Limit			3.6		V
Shutdown Voltage	VID - Shut Down Threshold		600		mV

**POWER MANAGEMENT**

**Pin Configurations**



**Ordering Information**

Part Number	Package	Temp. Range (T <sub>j</sub> )
SC2647SWTR <sup>(1)</sup>	SOIC-24	0 to 125 °C
SC2647TSTR <sup>(1)</sup>	TSSOP-24	0 to 125 °C
SC2647TSTRT <sup>(1,3)</sup>	TSSOP-24	0 to 125 °C
SC2647EVB <sup>(2)</sup>	Evaluation Board	

**Note:**

(1) Only available in tape and reel packaging. A reel contains 1000 devices for the SOIC-24 and 2500 devices for the TSSOP-24 package.

(2) Specify SOIC-24 or TSSOP-24 package.

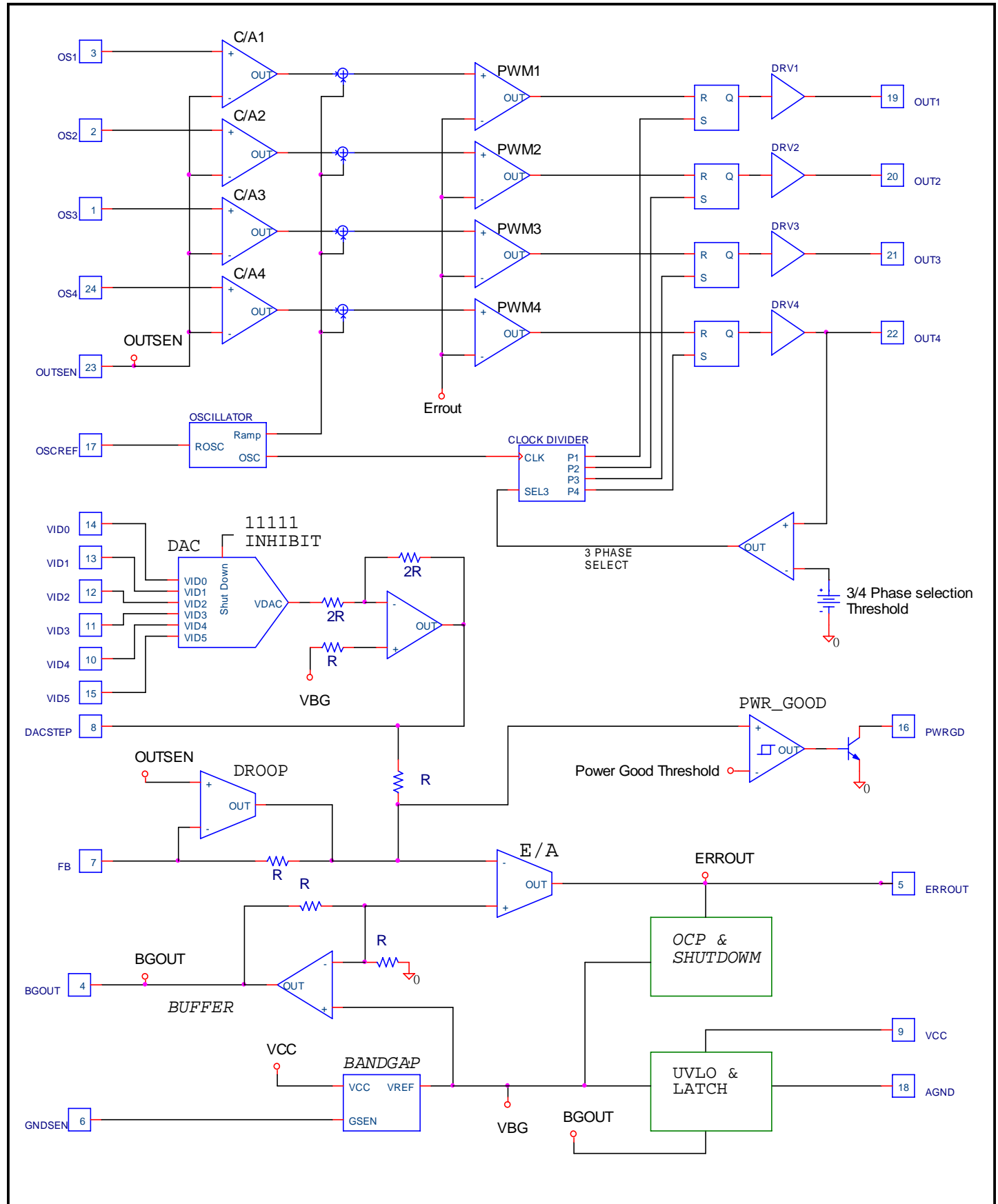
(3) Lead free product. This product is fully WEEE and RoHS compliant.

**Pin Descriptions**

Pin#	Pin Name	Pin Function
1	OS3	Current sense input.
2	OS2	Current sense input. Connect to OUTSEN for 2 phase operation.
3	OS1	Current sense input.
4	BGOUT	BG reference pin. Connect soft start cap from this pin to AGND.
5	ERROUT	Error-amplifier output. Connect compensation network to AGND.
6	GSENSE	Remote sense for GND.
7	FB	Feedback pin. Route FB and GENSE as differential pair to CPU.
8	DACSTEP	VID step speed. Connect a cap from this pin to AGND to filter DAC output.
9	VCC	Power supply for chip.
10~14	VID4 : 0	VID MSB to VID LSB.
15	VID5	12.5mV bit for VRD10.x. Pull it up to >2V and program the sink current to select VRM9 or K8 VID table.
16	PGOOD	Power good, Open collector output.
17	OSCREF	Oscillator frequency setting .Connect a resistor to AGND.
18	AGND	Clean ground for analog signals.
19	OUT1	PWM output1.
20	OUT2	PWM output2.
21	OUT3	PWM output3.
22	OUT4	PWM output4. Connect to VCC for 3 phase operation.
23	OUTSEN	Direct output sense.
24	OS4	Current sense input. Connect to OUTSEN for 2 or 3 phase operation.

**POWER MANAGEMENT**

**Block Diagram**



**POWER MANAGEMENT**
**Applications Information- Output Voltage**

VRM9.X Output Voltage					
Unless specified: 0 = GND; 1 = High (or Floating). $T_A = 25^\circ\text{C}$ , $V_{CC} = 5\text{V}$					Vout (V)
VID4	VID3	VID2	VID1	VID0	
1	1	1	1	1	OFF
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

**POWER MANAGEMENT**

**Applications Information- Output Voltag**

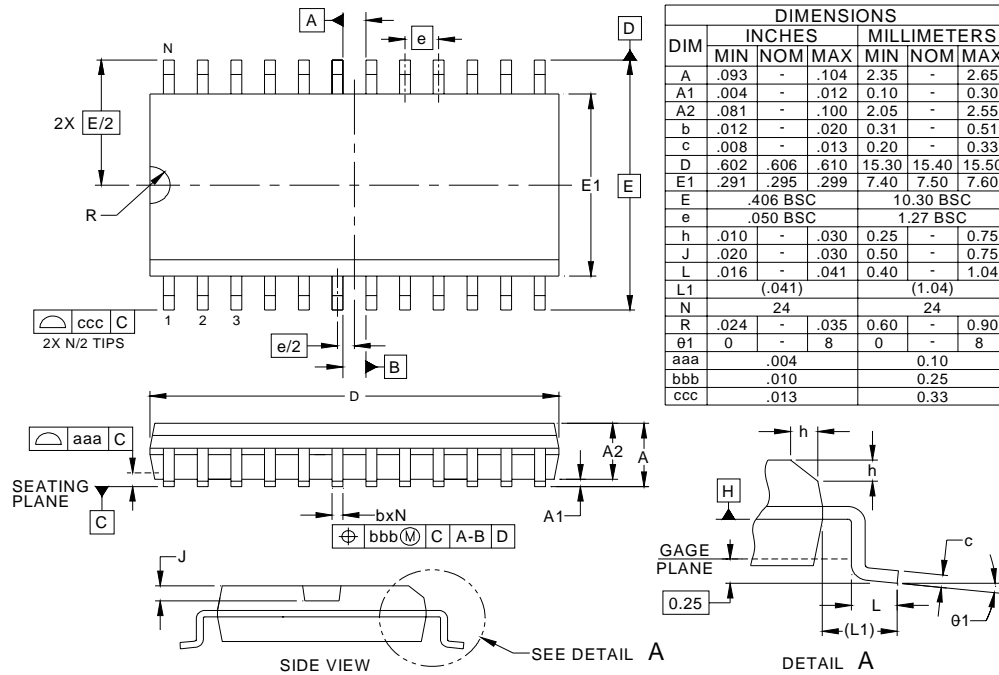
VRD10 Output Voltage							Vout (V)
Unless specified: 0 = GND; 1 = High. T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5V							
VID5	VID4	VID3	VID2	VID1	VID0		
0	0	1	0	1	0	0.8375	
1	0	1	0	0	1	0.8500	
0	0	1	0	0	1	0.8625	
1	0	1	0	0	0	0.8750	
0	0	1	0	0	0	0.8875	
1	0	0	1	1	1	0.9000	
0	0	0	1	1	1	0.9125	
1	0	0	1	1	0	0.9250	
0	0	0	1	1	0	0.9375	
1	0	0	1	0	1	0.9500	
0	0	0	1	0	1	0.9625	
1	0	0	1	0	0	0.9750	
0	0	0	1	0	0	0.9875	
1	0	0	0	1	1	1.0000	
0	0	0	0	1	1	1.0125	
1	0	0	0	1	0	1.0250	
0	0	0	0	1	0	1.0375	
1	0	0	0	0	1	1.0500	
0	0	0	0	0	1	1.0625	
1	0	0	0	0	0	1.0750	
0	0	0	0	0	0	1.0875	
1	1	1	1	1	1	OFF	
0	1	1	1	1	1	OFF	
1	1	1	1	1	0	1.1000	
0	1	1	1	1	0	1.1125	
1	1	1	1	0	1	1.1250	
0	1	1	1	0	1	1.1375	
1	1	1	1	0	0	1.1500	
0	1	1	1	0	0	1.1625	
1	1	1	0	1	1	1.1750	
0	1	1	0	1	1	1.1875	
1	1	1	0	1	0	1.2000	
0	1	1	0	1	0	1.2125	
1	1	1	0	0	1	1.2250	
0	1	1	0	0	1	1.2375	
1	1	1	0	0	0	1.2500	
0	1	1	0	0	0	1.2625	
1	1	0	1	1	1	1.2750	
0	1	0	1	1	1	1.2875	
1	1	0	1	1	0	1.3000	
0	1	0	1	0	0	1.3125	
1	1	0	1	0	1	1.3250	
0	1	0	1	0	1	1.3375	
1	1	0	1	0	0	1.3500	
0	1	0	1	0	0	1.3625	
1	1	0	0	1	1	1.3750	
0	1	0	0	1	1	1.3875	
1	1	0	0	1	0	1.4000	
0	1	0	0	1	0	1.4125	
1	1	0	0	0	1	1.4250	
0	1	0	0	0	1	1.4375	
1	1	0	0	0	0	1.4500	
0	1	0	0	0	0	1.4625	
1	0	1	1	1	1	1.4750	
0	0	1	1	1	1	1.4875	
1	0	1	1	1	0	1.5000	
0	0	1	1	1	0	1.5125	
1	0	1	1	0	1	1.5250	
0	0	1	1	0	1	1.5375	
1	0	1	1	0	0	1.5500	
0	0	1	1	0	0	1.5625	
1	0	1	0	1	1	1.5750	
0	0	1	0	1	1	1.5875	
1	0	1	0	1	0	1.6000	

**POWER MANAGEMENT**
**Applications Information- Output Voltag**

K-8 Output Voltage					
Unless specified: 0 = GND; 1 = High (or Floating). $T_A = 25^\circ\text{C}$ , $V_{CC} = 5\text{V}$					
VID4	VID3	VID2	VID1	VID0	$V_{OUT}$ (V)
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	OFF

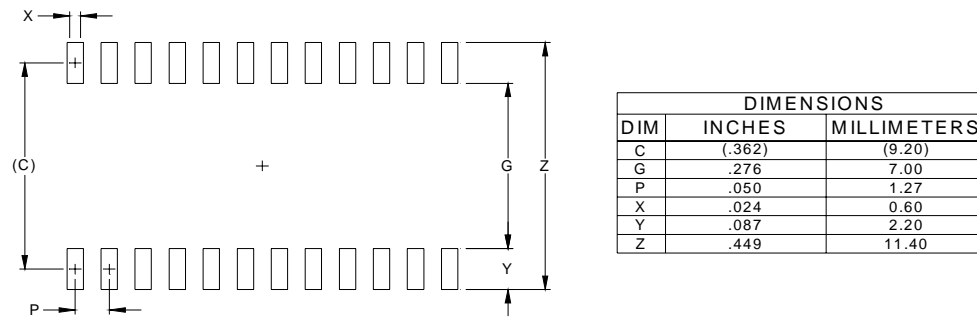
**POWER MANAGEMENT**

**Outline Drawing - SOIC-24**



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MS-013, VARIATION AD.

**Land Pattern - SOIC-24**



- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A, RLP NO. 307A.

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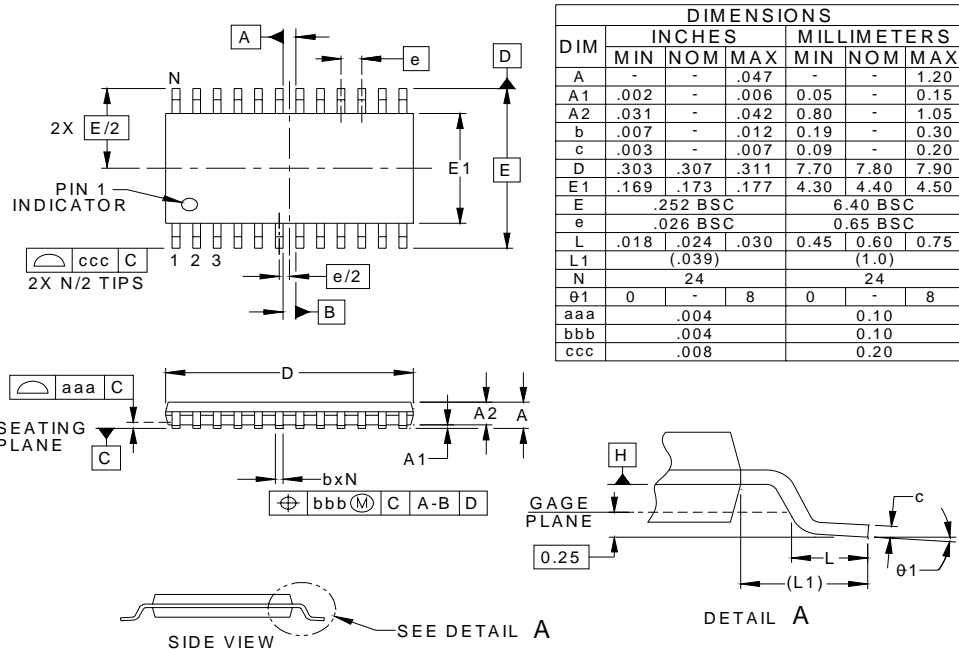
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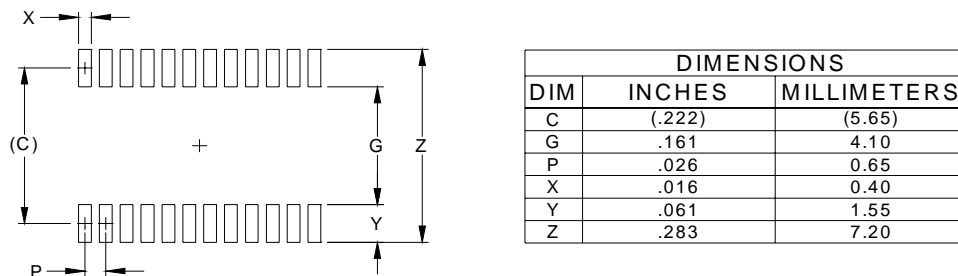
**POWER MANAGEMENT**

**Outline Drawing - TSSOP-24**



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS [-A-] AND [-B-] TO BE DETERMINED AT DATUM PLANE [-H-]
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MO-153, VARIATION AD.

**Land Pattern - TSSOP-24**



- NOTES:
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