



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
VCC, BSTL to GND	$V_{IN}$	-1.0 to 14	V
PGND to GND		± 0.5	V
PHASE to GND <sup>(1)</sup>		-0.5 to 18	V
BSTH to PHASE		14	V
Thermal Resistance Junction to Case	$\theta_{JC}$	45	°C/W
Thermal Resistance Junction to Ambient	$\theta_{JA}$	115	°C/W
Operating Temperature Range	$T_A$	0 to 70	°C
Maximum Junction Temperature	$T_J$	125	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	$T_{LEAD}$	300	°C

Note: (1) -1.5V to 20V for 25ns repetitive every cycle.

**Electrical Characteristics**

Unless specified:  $V_{CC} = 4.75V$  to  $12.6V$ ;  $GND = PGND = 0V$ ;  $FB = V_O$ ;  $V_{BSTL} = 12V$ ;  $V_{BSTH-PHASE} = 12V$ ;  $T_J = 25^\circ C$

Parameter	Conditions	Min	Typ	Max	Units
<b>Power Supply</b>					
Supply Voltage	VCC	4.2		12.6	V
Supply Current	EN = VCC		6	10	mA
Line Regulation	VO = 2.5V		0.5		%
<b>Error Amplifier</b>					
Gain (AOL)			35		dB
Input Bias			5	8	μA
<b>Oscillator</b>					
Oscillator Frequency	SC1102	170	200	230	kHz
	SC1102A	425	500	575	
Oscillator Max Duty Cycle		90	95		%
<b>MOSFET Drivers</b>					
DH Source/Sink	BSTH - DH = 4.5V, DH- PHASE = 2V	1			A
DL Source/Sink	BSTL - DL = 4.5V. DL - PGND. = 2V	1			A

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless specified:  $V_{CC} = 4.75V$  to  $12.6V$ ;  $GND = PGND = 0V$ ;  $FB = V_O$ ;  $V_{BSTL} = 12V$ ;  $V_{BSTH-PHASE} = 12V$ ;  $T_J = 25^\circ C$

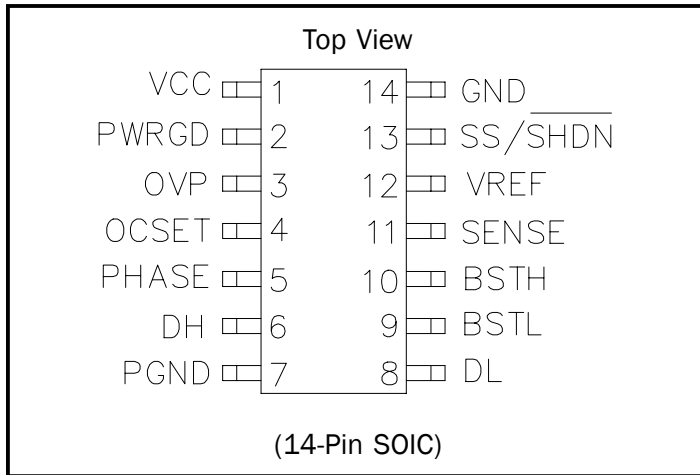
Parameter	Conditions	Min	Typ	Max	Units
<b>PROTECTION</b>					
OVP Threshold Voltage			20		%
OVP Source Current	$V_{OVP} = 3V$	10			mA
Power Good Threshold		88		112	%
Dead Time		45		100	ns
Over current Set Isink	$2.0V \leq V_{OCSET} \leq 12V$	180	200	220	$\mu A$
<b>Reference</b>					
Reference Voltage	$0^\circ C$ to $70^\circ C$	1.252	1.265	1.278	V
Accuracy		-1		+1	%
<b>Soft Start</b>					
Charge Current	$V_{SS} = 1.5V$	8.0	10	12	$\mu A$
Discharge Current	$V_{SS} = 1.5V$		1.5		$\mu A$

**NOTES:**

- (1) Specification refers to application circuit (Figure 1).
- (2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

## POWER MANAGEMENT

### Pin Configuration



### Ordering Information

Device <sup>(1)</sup>	Frequency	Package
SC1102CS.TR	200kHz	SO-14
SC1102CSTRT <sup>(2)</sup>		
SC1102ASTR	500kHz	
SC1102ASTRT <sup>(2)</sup>		
SC1102EVB	Evaluation Board	

#### Notes:

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

### Pin Descriptions

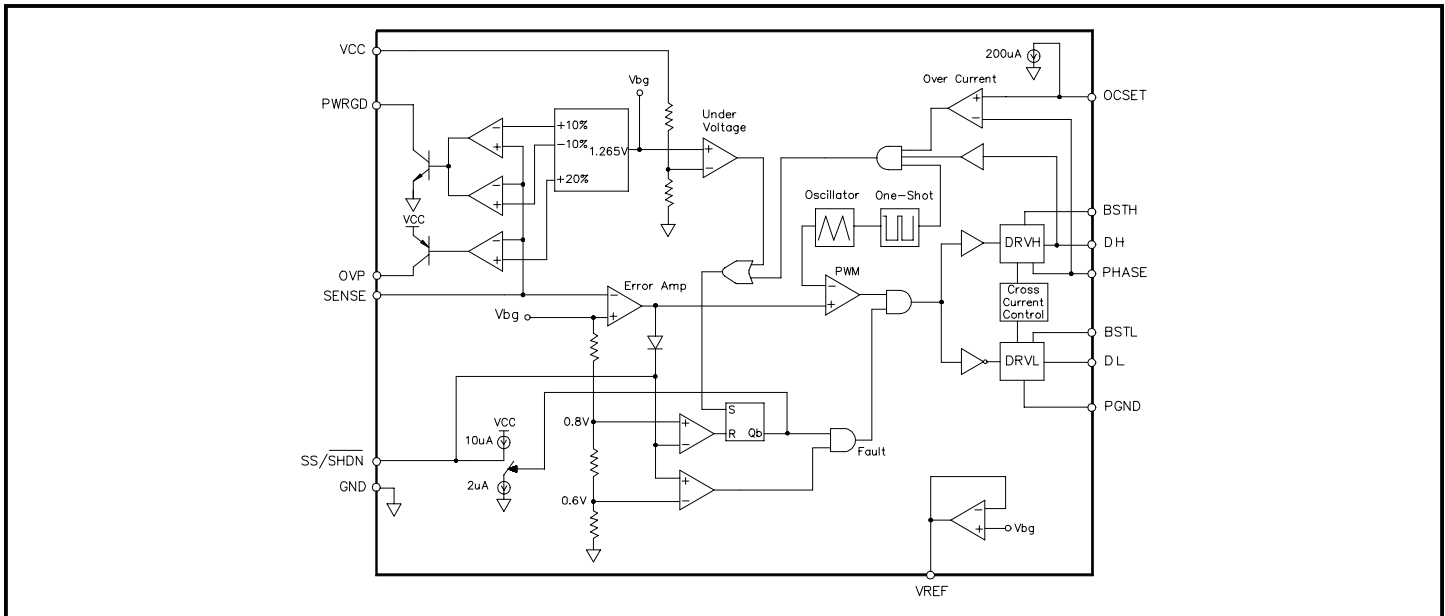
Pin #	Pin Name	Pin Function
1	VCC	Chip supply voltage
2	PWRGD	Logic high indicates correct output voltage
3	OVP	Over voltage protection.
4	OCSET	Sets the converter overcurrent trip point
5	PHASE	Input from the phase node between the MOSFET'S
6	DH	High side driver output
7	PGND	Power ground
8	DL	Low side driver output
9	BSTL	Bootstrap, low side driver.
10	BSTH	Bootstrap, high side driver.
11	SENSE	Voltage sense input
12	VREF	Buffered band gap voltage reference.
13	SS/ <u>SHDN</u>	Soft start. A capacitor to ground sets the slow start time.
14	GND	Signal ground

#### NOTE:

(1) All logic level inputs and outputs are open collector TTL compatible.

## POWER MANAGEMENT

### Block Diagram



### Applications Information - Theory of Operation

#### Synchronous Buck Converter

Primary  $V_{CORE}$  power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including “Power Good” flag, shut-down, and cycle-by-cycle current limit.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed-bandgap voltage reference (See Fig.

- 1). The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200kHz/500kHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. The non-inverting input of the comparator receives its input voltage from the error amplifier. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH

low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET driver outputs, hence lowering the output voltage.

#### Under Voltage Lockout

The under voltage lockout circuit of the SC1102 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if  $V_{CC}$  falls below 4.1V. Normal operation resumes once  $V_{CC}$  rises above 4.2V.

#### Over-Voltage Protection

The over-voltage protection pin (OVP) is high only when the voltage at SENSE is 20% higher than the target value programmed by the external resistor divider. The OVP pin is internally connected to a PNP’s collector.

#### Power Good

The power good function is to confirm that the regulator outputs are within +/-10% of the programmed level. PWRGD remains high as long as this condition is met. PWRGD is connected to an internal open collector NPN transistor.

## POWER MANAGEMENT

### Applications Information (Cont.)

#### Soft Start

Initially,  $\overline{\text{SS/SHDN}}$  sources  $10\mu\text{A}$  of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on  $\overline{\text{SS/SHDN}}$ . This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

#### $R_{\text{DS(ON)}}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the  $V_{\text{CC}}$  supply to OCSET. The voltage drop across this resistor is due to the  $200\mu\text{A}$  internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFETs off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switch turns off and  $\overline{\text{SS/SHDN}}$  starts to sink  $2\mu\text{A}$ . When  $\overline{\text{SS/SHDN}}$  reaches  $0.8\text{V}$ , it then starts to source  $10\mu\text{A}$  and a new cycle begins.

#### Hiccup Mode

During power up, the  $\overline{\text{SS/SHDN}}$  pin is internally pulled low until VCC reaches the undervoltage lockout level of  $4.2\text{V}$ . Once  $V_{\text{CC}}$  has reached  $4.2\text{V}$ , the  $\overline{\text{SS/SHDN}}$  pin is released and begins to source  $10\mu\text{A}$  of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from  $1\text{V}$  to  $2\text{V}$  at a fixed frequency of  $200\text{kHz}/500\text{kHz}$ , switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about  $2.2\text{V}$ .

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. The PHASE node is sampled only once per cycle during the valley of the triangular oscillator. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the  $\overline{\text{SS/SHDN}}$  pin begins to sink  $2\mu\text{A}$ . The soft-start voltage will begin to decrease as the  $2\mu\text{A}$  of current discharges the external capacitor. When the soft-start voltage reaches  $0.8\text{V}$ , the  $\overline{\text{SS/SHDN}}$  pin will begin to source  $10\mu\text{A}$  and begin to charge the external capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the  $\overline{\text{SS/SHDN}}$  pin will again begin to sink  $2\mu\text{A}$ . This cycle will continue indefinitely until the over-current condition is removed.

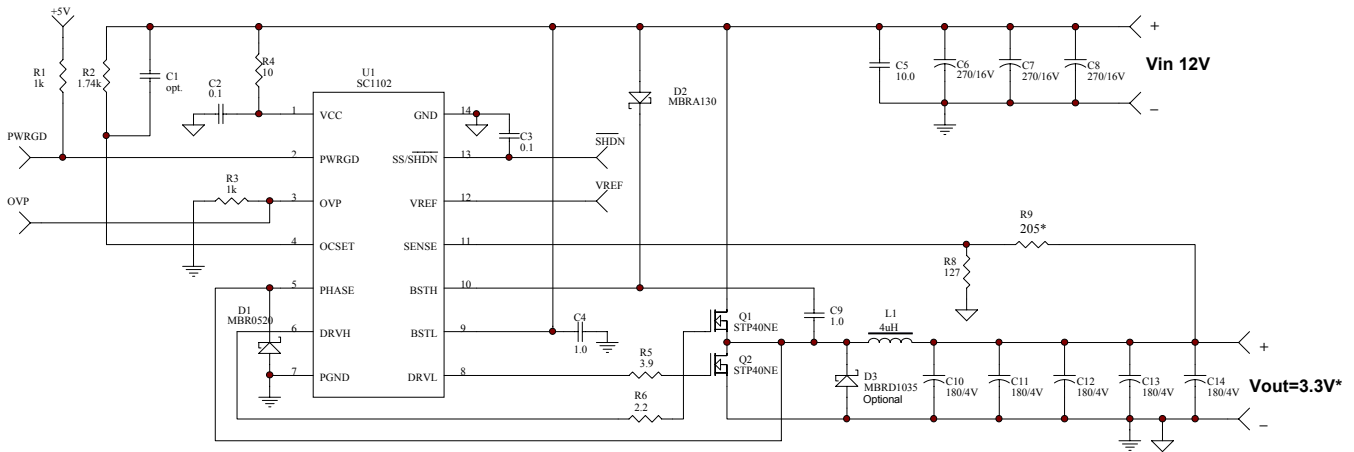
In conclusion, below is shown a typical “12V Application Circuit” which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D1. This circuit is very useful in cases where only input power of  $12\text{V}$  is available.

In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to PGND.

**POWER MANAGEMENT**

**Application Circuit**

Typical 12V Application Circuit with Bootstrapped BSTH



NOTE:  
\*)  $V_{out} = 1.265 \times (1 + R9/R8)$

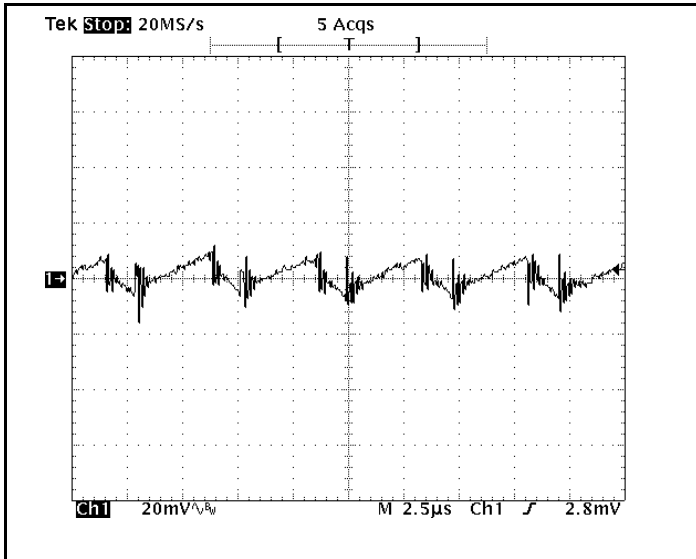
## POWER MANAGEMENT

### Typical Characteristics

#### Output Ripple Voltage

Ch1: Vo\_rpl

1.  $V_{IN} = 5V$ ;  $V_O = 3.3V$ ;  $I_{OUT} = 12A$

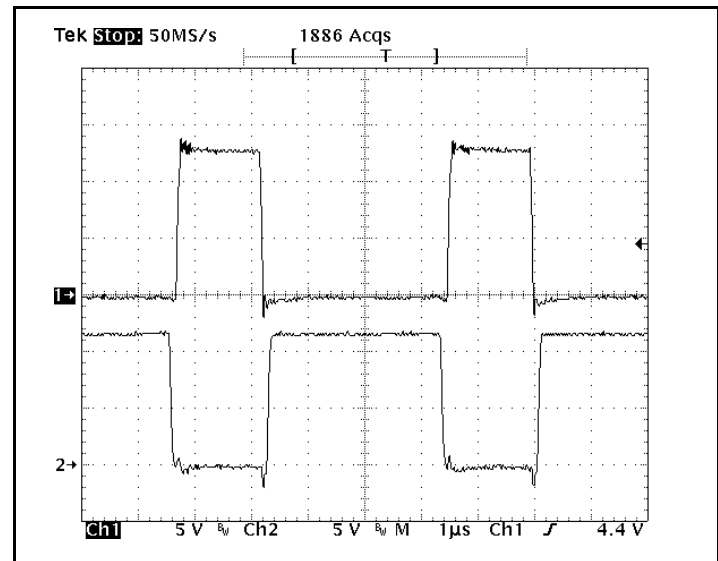
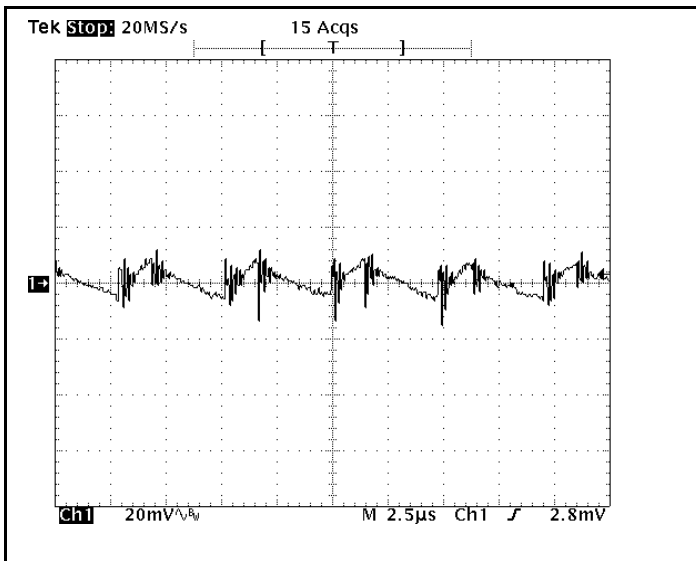
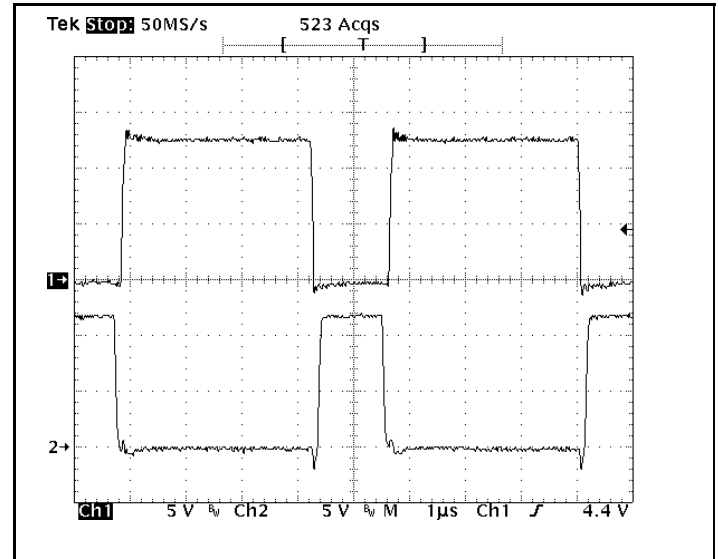


Wave forms are shown for SC1102 and are similar for SC1102A but at a higher frequency.

#### Gate Drive Waveforms

Ch1: Top FET

Ch2: Bottom FET



Ch1: Vo\_rpl

2.  $V_{IN} = 5V$ ;  $V_{OUT} = 1.3V$ ;  $I_{OUT} = 12A$

Ch1: Top FET

Ch2: Bottom FET

**POWER MANAGEMENT**

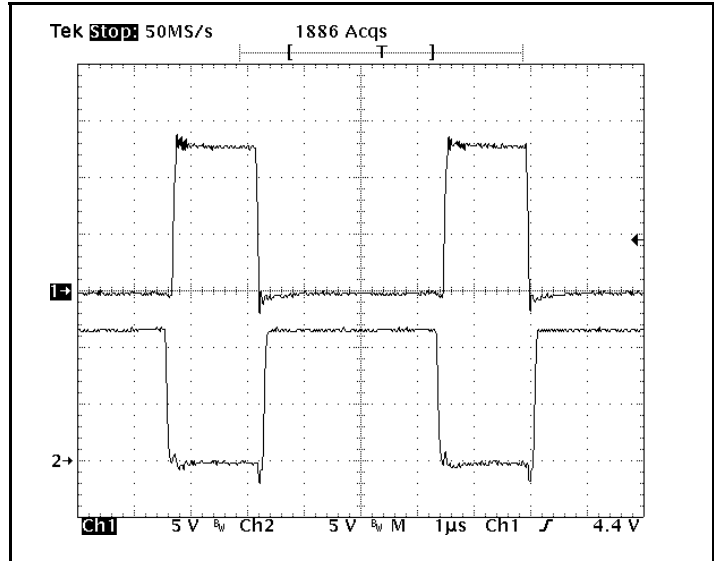
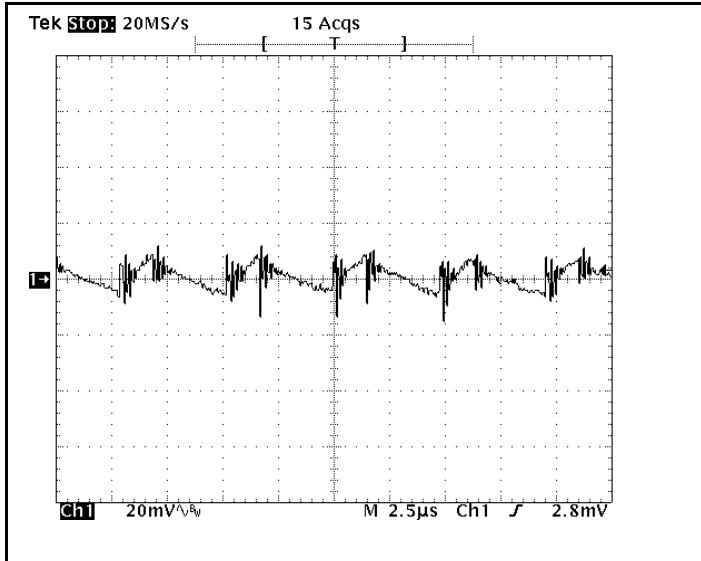
**Typical Characteristics (Cont.)**

Ch1: Vo\_rpl

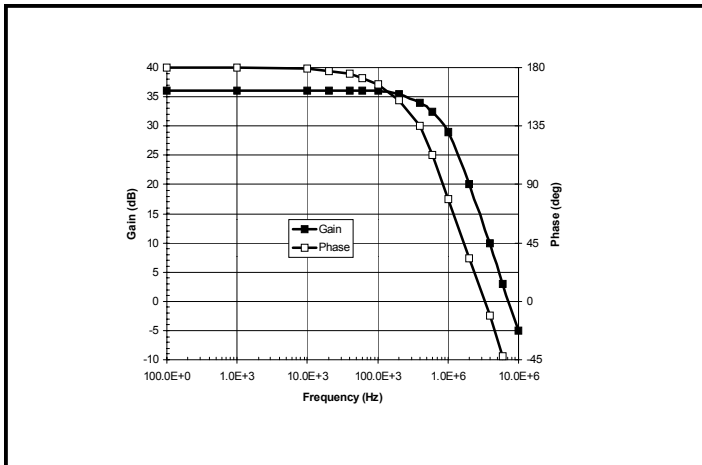
2.  $V_{IN} = 5V$ ;  $V_{OUT} = 1.3V$ ;  $I_{OUT} = 12A$

Ch1: Top FET

Ch2: Bottom FET



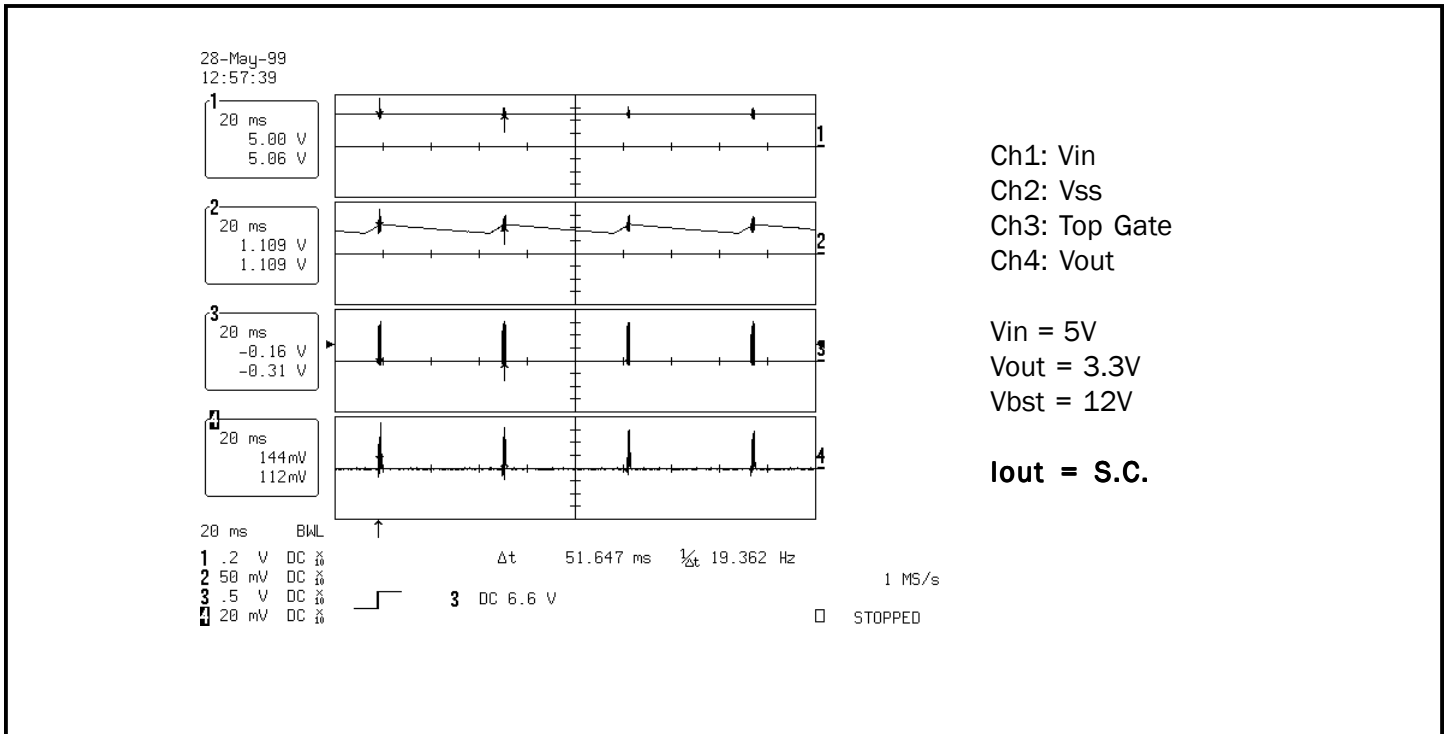
**Error Amplifier, Gain and Phase**



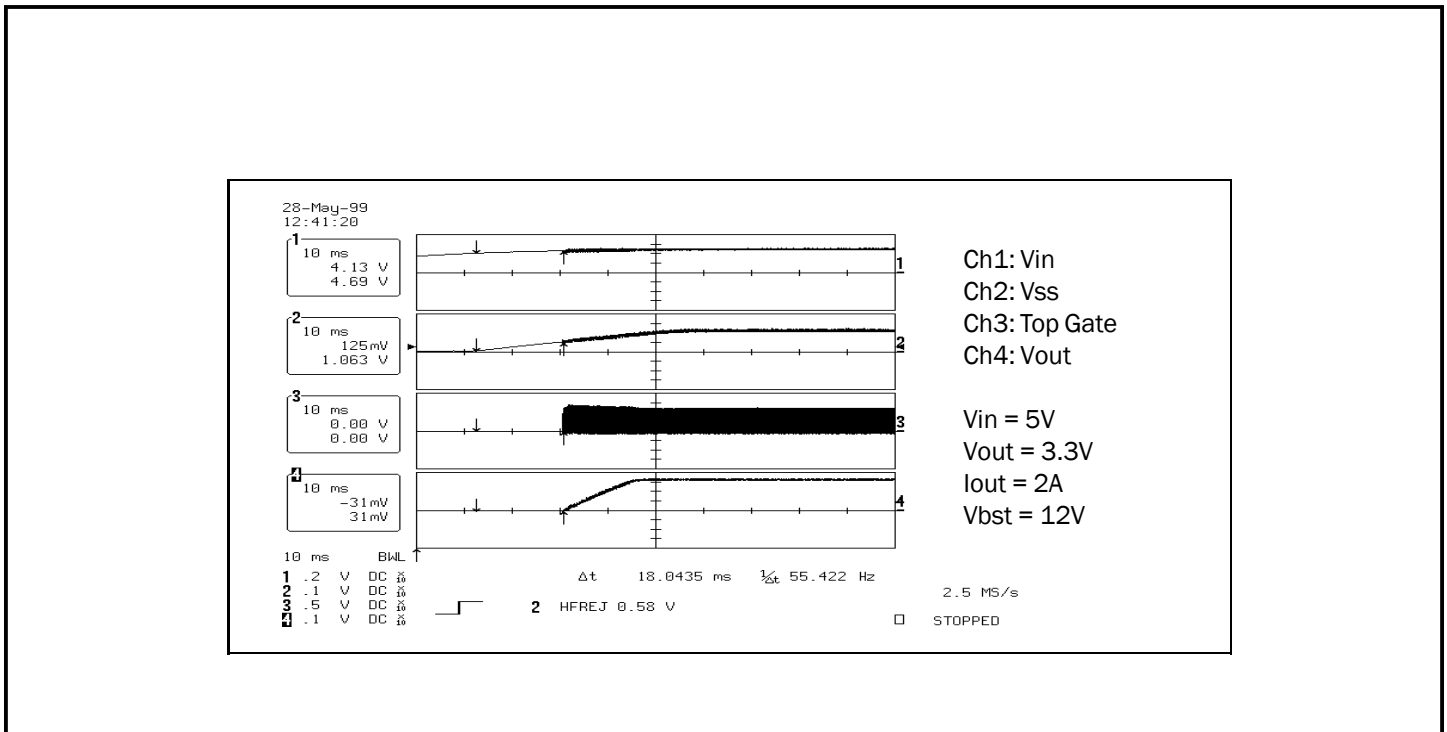
**POWER MANAGEMENT**

**Typical Characteristics (Cont.)**

**Hiccup Mode**

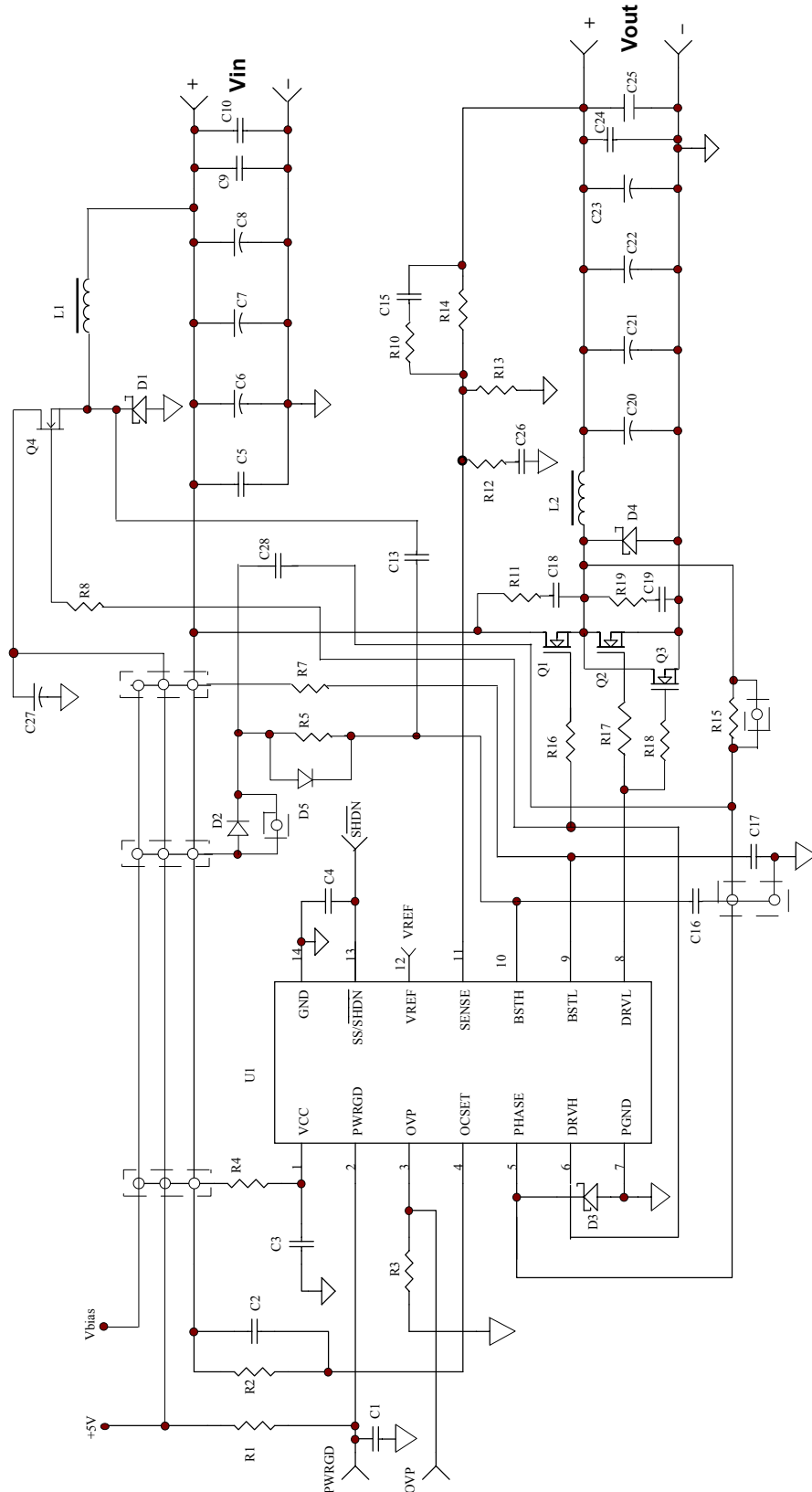


**Start Up Mode**



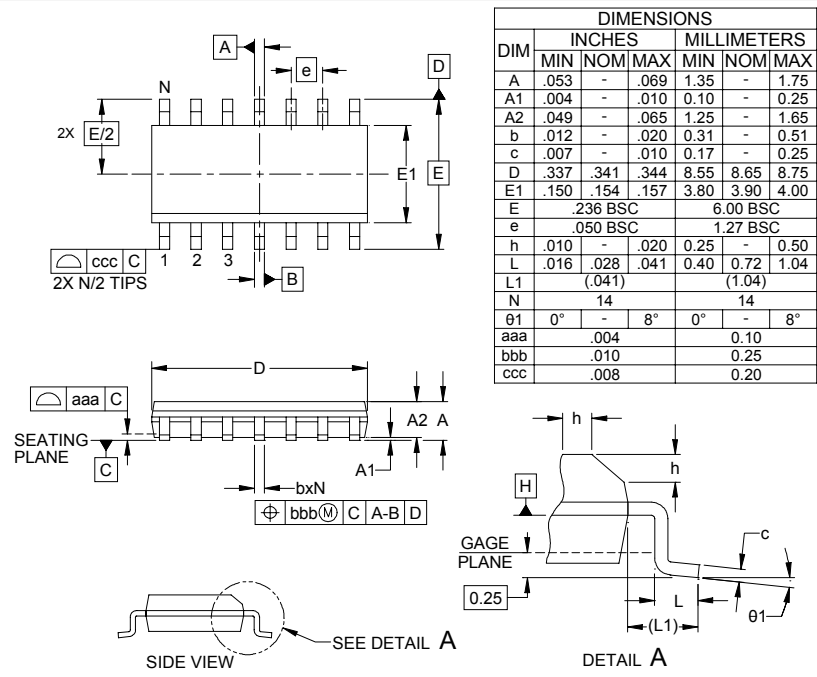
**POWER MANAGEMENT**

**Evaluation Board Schematic**



## POWER MANAGEMENT

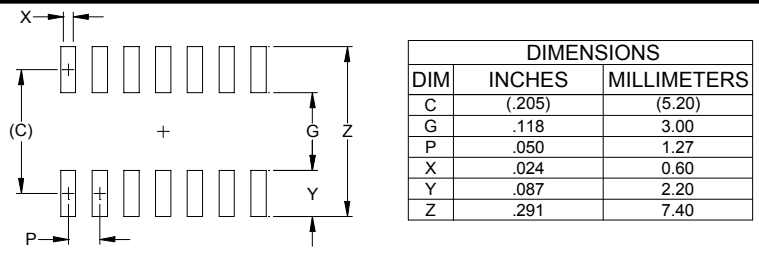
### Outline Drawing - SOIC - 14



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.337	.341	.344	8.55	8.65	8.75
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **A-** AND **B-** TO BE DETERMINED AT DATUM PLANE **H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MS-012, VARIATION AB.

### Land Pattern - SOIC - 14



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A, RLP NO. 302A.

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