

AN 1200.04

Application Note

RF Design Guidelines:  
PCB Layout and Circuit Optimization

# 1 Table of Contents

1	Table of Contents.....	2
1.1	Index of Figures.....	2
1.2	Index of Tables.....	2
2	Introduction.....	3
3	General PCB Layout Techniques.....	4
3.1	4-Layer Designs.....	4
3.2	2-Layer Designs.....	5
3.3	PCB Transmission Lines.....	6
3.4	Current Loops and Decoupling.....	7
3.5	PCB Parasitics.....	7
4	RF Device PCB Layout and Optimization.....	9
4.1	Thermal Relief Pad.....	9
4.2	VCO and Loop Filter.....	9
4.2.1	PCB Layout.....	9
4.2.2	Optimization.....	11
4.3	Transmitter Circuit.....	12
4.3.1	Optimization.....	12
4.3.2	PCB Layout.....	16
4.4	Receiver LNA Circuit.....	16
4.4.1	PCB Layout.....	16
4.4.2	Circuit Optimization.....	17
5	Passive Components.....	20
5.1	Capacitors.....	20
5.2	Inductors.....	21

## 1.1 Index of Figures

Figure 1:	Semtech Transceiver Architecture.....	3
Figure 2:	4-Layer PCB Build-Up.....	4
Figure 3:	2-Layer Reference Design.....	5
Figure 4:	PCB Microstrip Trace.....	6
Figure 5:	Circuit Decoupling and Current Loop Minimization.....	7
Figure 6:	PCB Via.....	8
Figure 7:	Multiple Via Connection of Thermal Pad.....	9
Figure 8:	VCO Tank Circuit Layout.....	10
Figure 9:	PLL Loop Filter.....	10
Figure 10:	Semtech Loop Filter Configurations.....	11
Figure 11:	TX Matching Network.....	12
Figure 12:	Measurement of Optimum Load Impedance Presented to the Transmitter.....	13
Figure 13:	Design of Pi-Section Filter.....	14
Figure 14:	Impedance Transformation.....	15
Figure 15:	Optimized Matching Circuit.....	15
Figure 16:	Transmitter Section PCB Layout.....	16
Figure 17:	LNA Matching Network.....	16
Figure 18:	LNA PCB Layout.....	17
Figure 19:	Measurement and Optimization of the LNA Matching network.....	18
Figure 20:	Optimized LNA Matching Network Input Reflection Coefficient.....	18
Figure 21:	I and Q Channel Output Signals.....	19
Figure 22:	Equivalent Circuit of a Multilayer Ceramic Capacitor.....	20
Figure 23:	Inductor Equivalent Circuit.....	21

## 1.2 Index of Tables

Table 1:	Optimum Transmitter Load Impedance.....	13
Table 2:	Typical I, Q Signal Amplitudes.....	19
Table 3:	Typical Decoupling Capacitor Values.....	20
Table 4:	Typical Inductor Types.....	22

## 2 Introduction

The purpose of this document is to describe RF PCB design guidelines and circuit optimization techniques to enable the designer to implement successful, right-first-time, PCB layouts and to ensure trouble free circuit optimization, using the same criteria as those employed by Semtech for the reference designs of the XE/SX1200 family of RF ISM band integrated circuits.<sup>1</sup>

This application note describes step by step techniques for ensuring the correct PCB layout and subsequent design optimization steps for each circuit block of the RF integrated circuit architecture.

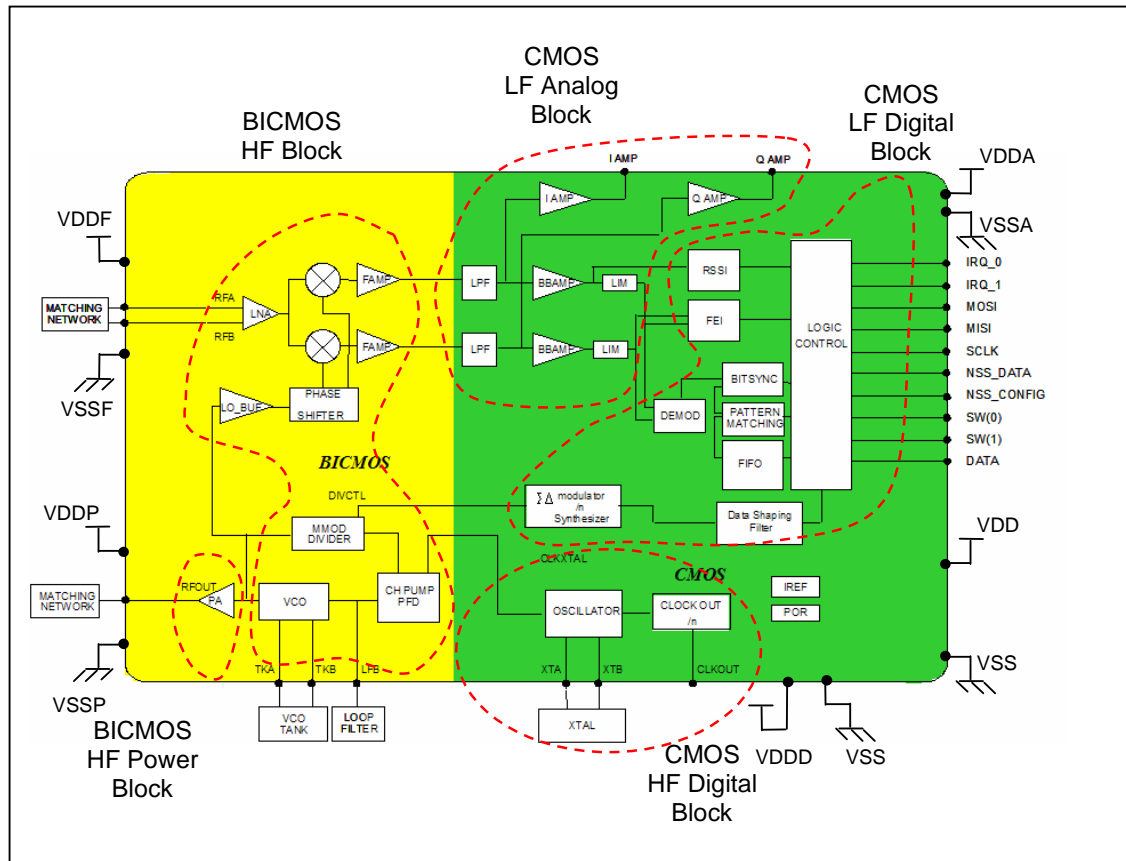


Figure 1: Semtech Transceiver Architecture

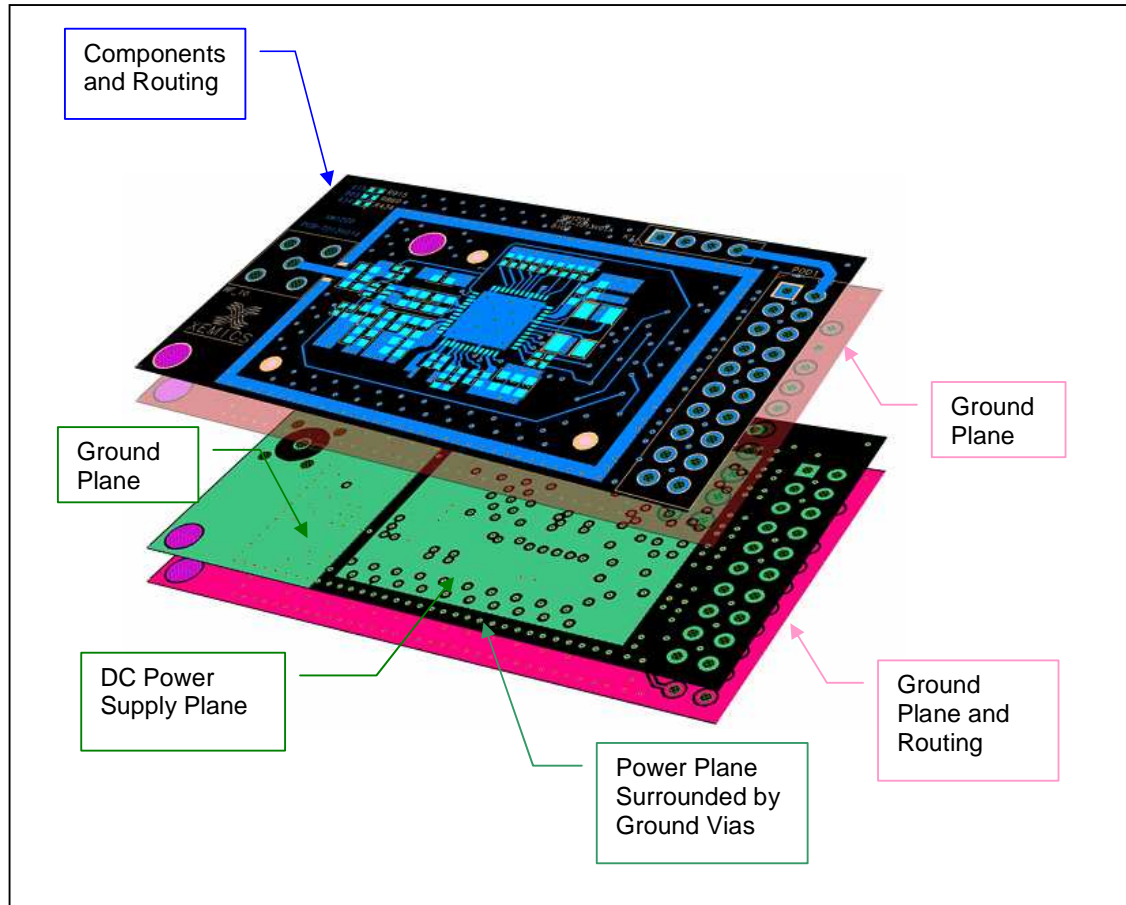
<sup>1</sup> Reference design files for Semtech's XE/SX1200 RF ISM band ICs can be obtained by contacting [sales@semtech.com](mailto:sales@semtech.com)

### 3 General PCB Layout Techniques

Semtech offers both 4-layer and 2-layer reference designs for its family of RF ICs for FR4 PCB material.

#### 3.1 4-Layer Designs

The advantages of 4-layer designs over 2-layer designs is that the former allows for distributed RF decoupling of a DC power plane sandwiched between two layers of predominantly ground plane, as illustrated below in Figure 2:



**Figure 2: 4-Layer PCB Build-Up**

Placing a distributed power plane between 2 ground plane layers enables an evenly distributed RF decoupling capacitance between the supply and ground. In addition, the power plane provides a very low impedance trace at radio frequencies.

The power plane should be surrounded by a ground trace or vias that connect the two ground traces together, thus preventing any radiated emissions at the board edge. From the above figure, the power plane is suppressed at the final stage of the TX matching network to prevent any parasitic coupling caused by radiated and reflected energy at this stage.

A 4 or multilayer PCB layout lends itself should an additional RF Power Amplifier be required (for example to take advantage of the transmit power allowances of FCC Part 15.247). Generally speaking, the power supply of the PA will be the (unintentionally) noisiest PCB trace. A multi-layer approach allows for a separate low impedance power supply plane for the PA, while allowing for a continuous grounding strategy. Alternatively, separate ground and power supply layers that can be

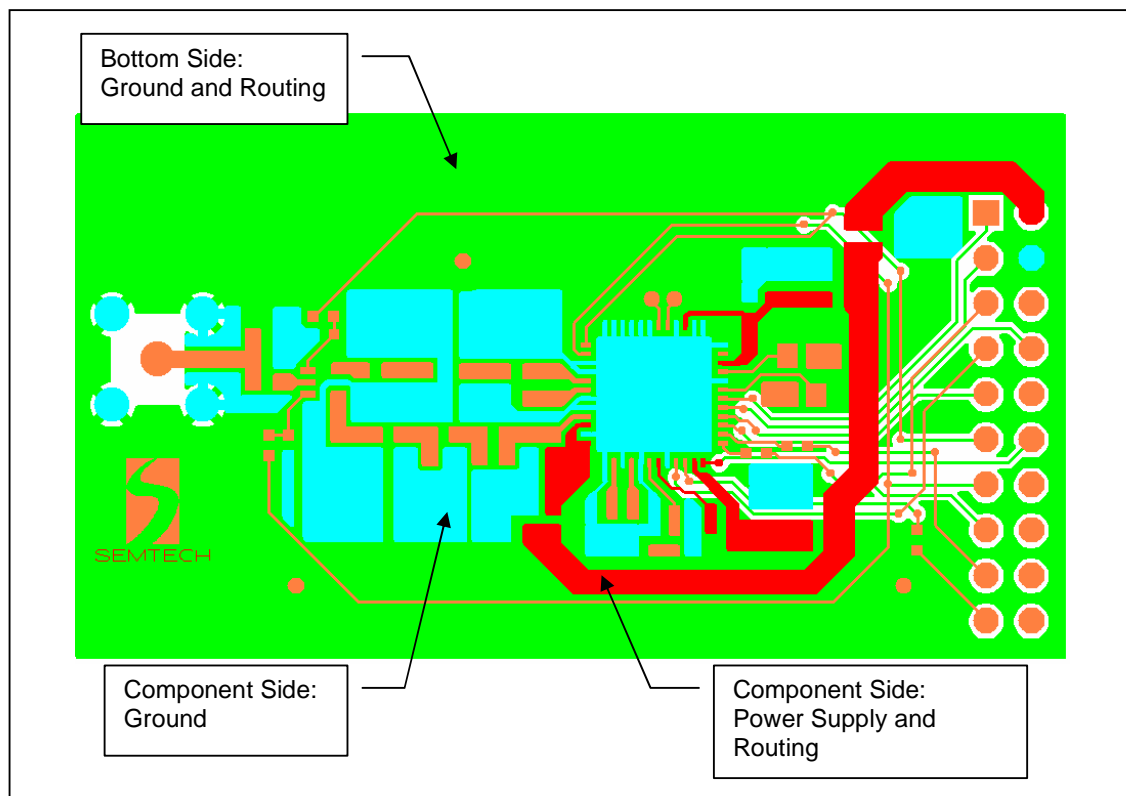
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connected to common star points can be employed, although care should be taken to ensure that any return current paths are not routed under sensitive RF circuit blocks. While a common low-impedance ground plane offers a robust, practical solution, there is no generic “right solution” and the power supply and grounding philosophy employed will depend upon the application.

Another advantage of a 4-layer design is that for an overall PCB thickness of 1.6mm (0.063”), the gap between the PCB component and routing layer and the first ground plane layer allows for distributed Microstrip traces to be employed. Similarly for RF routing on the layer between the ground planes or well-decoupled power planes, Stripline techniques can be employed to ensure that traces have the required characteristic impedance (typically 50Ω). Microstrip traces are described in Section 3.3.

### 3.2 2-Layer Designs

2-layer designs typically require a little more care with the PCB routing but can be successfully implemented, as illustrated below in Figure 3:



**Figure 3: 2-Layer Reference Design**

Note that the power supply trace on the component is made quite thick so as to present as low as impedance trace as possible. Large areas of ground on this side of the board provide a low impedance path for decoupling.

Wherever possible the bottom (copper) side of the board should allow for a solid ground plane under the RF circuitry.

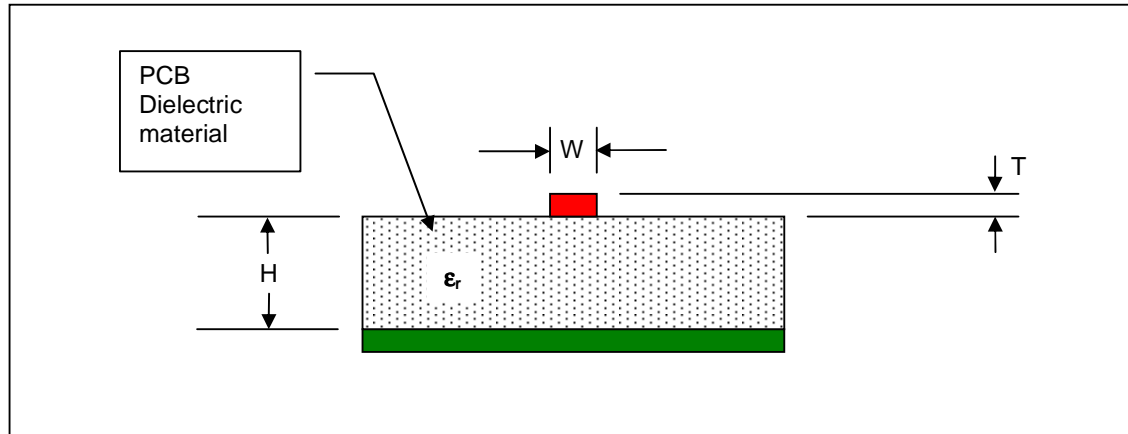
A 2-layer PCB will be cheaper to manufacture than a 4-layer PCB. However, to implement Microstrip or Stripline transmission lines the PCB thickness should not exceed 0.8mm - 1.00mm (0.031” - 0.039”), since the width of the transmission line trace will become rather large. PCBs of this thickness do not generally lend themselves to large sizes because of their fragility.

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To overcome this problem with 2-layer designs, try and keep RF circuit traces as short as possible ( $< \lambda/30$ ) or for longer traces taper the trace so that the apart from the connection to any multi-footprint component, the trace appears as close to  $50 \Omega$  as possible.

### 3.3 PCB Transmission Lines

Figure 4, below illustrates an example of a PCB trace on the component or top side of the board that is isolated by the PCB dielectric material (typically FR4) from the ground plane layer. From knowledge of the physical properties of the PCB it is possible to construct a transmission line trace with the desired characteristic impedance.



**Figure 4: PCB Microstrip Trace**

To calculate the required width of the PCB trace,  $W$ , it is first necessary to calculate the effective dielectric constant,  $\epsilon_{eff}^2$ . The effective dielectric constant is required because part of the field generated by the conductor will exist in air ( $\epsilon = 1$ ) and part in the dielectric material. Assuming that the thickness of the trace,  $T$ , is small compared to the height of the dielectric ( $T/H < 0.005$ ), then  $\epsilon_{eff}$  can be calculated using the following formulae:

$$\left(\frac{W}{H}\right) < 1: \quad \epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[ \left(1 + 12\left(\frac{H}{W}\right)\right)^{\frac{1}{2}} + 0.04\left(1 - \left(\frac{W}{H}\right)\right)^2 \right] \quad (3.1)$$

$$\left(\frac{W}{H}\right) > 1: \quad \epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + 12\left(\frac{H}{W}\right)\right)^{\frac{1}{2}} \quad (3.2)$$

With  $\epsilon_{eff}$  calculated in (5.1) or (5.2) above, the characteristic impedance of a Microstrip line can be calculated as follows:

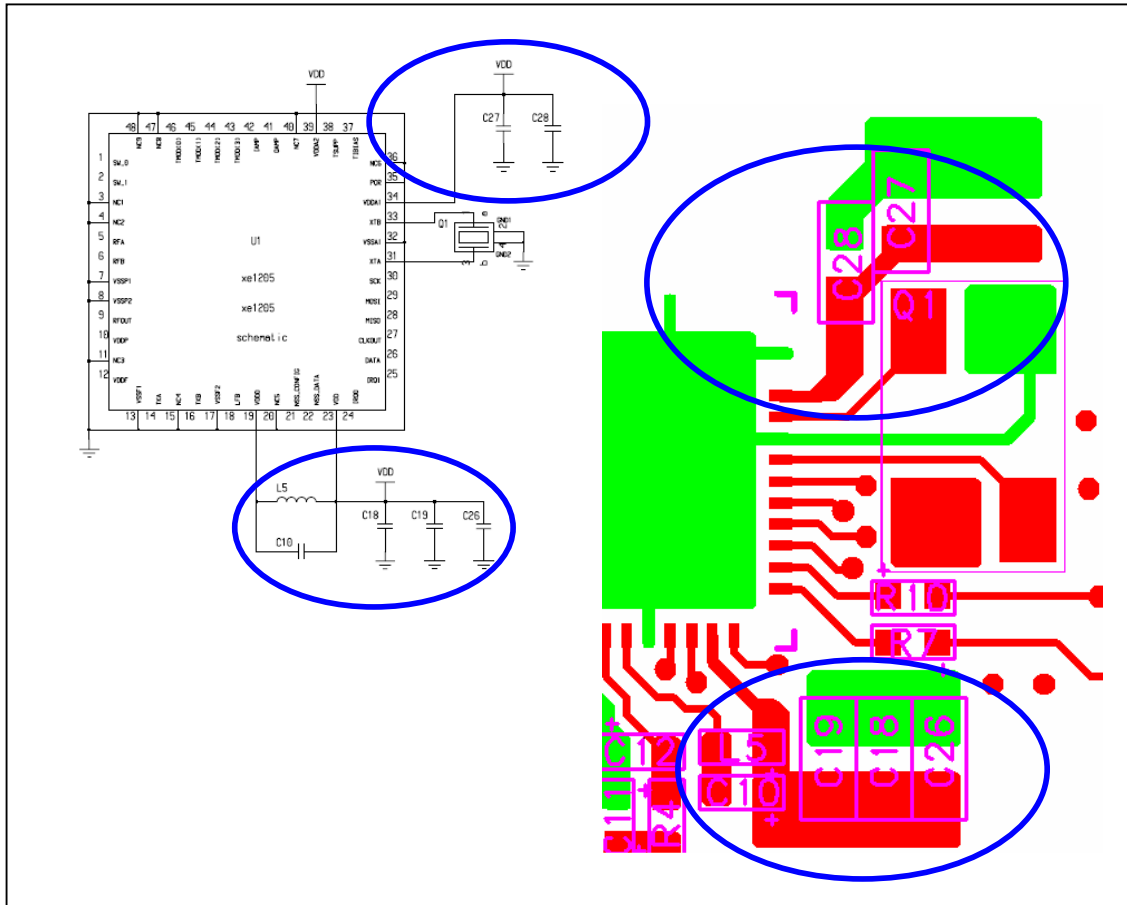
$$\left(\frac{W}{H}\right) < 1: \quad Z_0 = \frac{60}{\sqrt{\epsilon_{eff}}} * \ln\left(8\frac{H}{W} + 0.25\frac{W}{H}\right) \quad (3.3)$$

$$\left(\frac{W}{H}\right) > 1: \quad Z_0 = \frac{\frac{120\pi}{\sqrt{\epsilon_{eff}}}}{\frac{W}{H} + 1.393 + 0.667 \ln\left(\frac{W}{H} + 1.444\right)} \quad (3.4)$$

<sup>2</sup> I. J. Bahl and D. K. Trvedi, "A Designer's Guide to Microstrip Line", *Microwaves*, May 1977

### 3.4 Current Loops and Decoupling

Minimize current loops on PCB layouts by decoupling as close to the port being decoupled to ground as possible. Try and avoid capacitive coupling by ensuring that each circuit block or port has its own decoupling capacitor. Ensure that each decoupling capacitor has its own via connection to ground. As a rule of thumb, components should not share vias.



**Figure 5: Circuit Decoupling and Current Loop Minimization**

Figure 5 above illustrates examples of PCB layouts to minimize current loops. The power supplies are decoupled as close to the supply pin of the IC as possible to a localized ground pad on the top layer that connected to the main ground plane layer through multiple vias. In the above example L5, C10 form a resonant tuned circuit at the LO frequency to minimize the coupling of TX related sidebands being injected into the power supply as AM noise and generating FM noise at the transmitter output.

By minimizing current loops and through careful and considered decoupling it is possible to avoid noise from the noisy circuit blocks, such as the digital blocks, PLL frequency synthesizer and reference oscillator circuit being coupled into highly sensitive circuit blocks such as the LNA and VCO.

### 3.5 PCB Parasitics

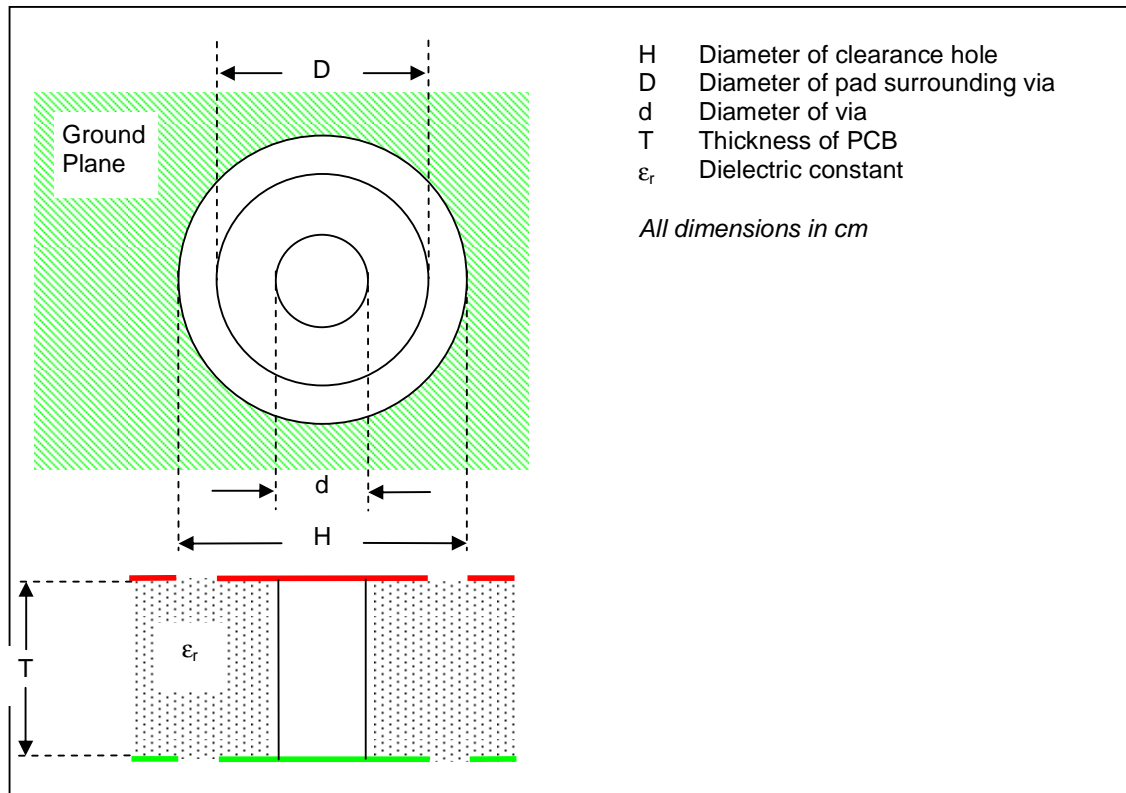
An area that is often over looked during PCB layout is the electrical characteristics of the PCB material itself, component traces and vias. The electrical characteristics of the PCB used to physically mount and connect the circuit components in a high frequency RF product can have a significant impact on the performance of that product.<sup>3</sup>

<sup>3</sup> Geoff Smithson, "Practical RF Printed Circuit Board Design", Plextek Ltd ([www.plextek.co.uk](http://www.plextek.co.uk))

“PCB Parasitics” refers to any physical attribute of the board that affects the performance of the circuit. At RF it can be seen that a long signal trace will have inductance associated with it, while a pad over an area of ground plane or power plane will have an associated capacitance.

An often overlooked PCB parasitic component is the via, used to connect one PCB layer to another.

Consider a standard PCB through-hole via, illustrated below in Figure 6.



**Figure 6: PCB Via**

The via will have an associated parasitic parallel capacitance and inductance, that will form a parallel resonant circuit. As a rule of thumb, these parasitic components can be calculated as follows:

$$\text{Inductance, } L = 2T \left[ \ln \frac{4T}{d} + 1 \right] \text{ nH} \quad (3.5)$$

$$\text{Capacitance, } C = \frac{0.55\epsilon_r T D}{H - D} \text{ pF} \quad (3.6)$$

Typically for a 1.6mm thickness PCB material, a single via can add 1.2nH of inductance and 0.5pF of capacitance, depending upon the via dimensions and PCB dielectric material, although the effects can be minimized by ensuring that the inter-via spacing is of the order of  $\lambda/30$ .

Sometimes the knowledge of the physical properties of the PCB can be used to the advantage of the design engineer. For example, an inductance derived from a PCB trace will offer much greater repeatability than a commercially available component.

## 4 RF Device PCB Layout and Optimization

### 4.1 Thermal Relief Pad

The thermal relief pad on the underside of Semtech RF devices provides both thermal relief and a solid ground reference to the chip. This pad should be ideally connected to a component side ground connection which in turn is connected to the main ground plane layer by multiple vias.

Figure 7 illustrates the multiple via (or “well stitched”) connection of the thermal relief pad to the main (inner) ground layer. The multiple vias ensure that the total parasitic inductance associated with the vias is minimized by several parallel connections. In addition, distributed vias ensure an even thermal distribution.

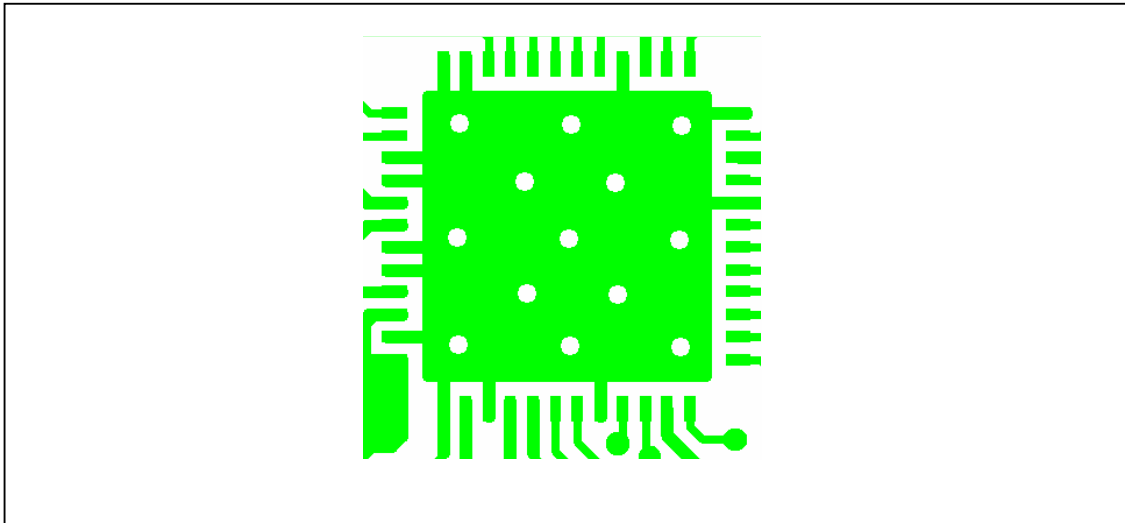


Figure 7: Multiple Via Connection of Thermal Pad

### 4.2 VCO and Loop Filter

#### 4.2.1 PCB Layout

The external VCO tank circuit of the XE1200 series transceiver ICs consists of an external L (and in some instances a parallel capacitor) across a differential input. Hence the PCB layout should endeavor to respect the symmetry of this port.

As discussed in Section 3.5 above, PCB trace parasitics can influence circuit operation and act as unintentional radiators. To minimize radiation from the VCO circuit, keep the traces as short as possible.

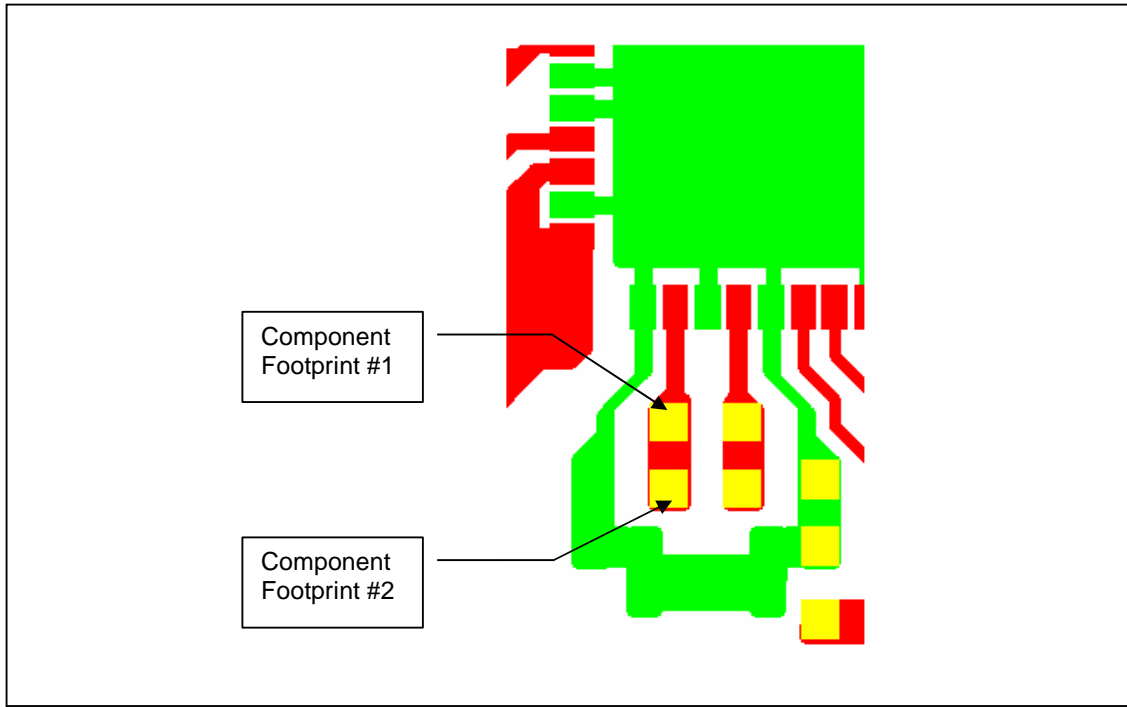
Figure 8, below, illustrates the symmetrical PCB layout of the XE1200 series VCO tank. Note that the traces are kept as short as possible, and the entire circuit is enclosed within a ground or guard band. This ground trace both minimizes radiation from the VCO as well as preventing noise being injected directly into the VCO itself.

Note that the PCB trace allows for five possible combinations of components:

- A single inductor on footprint #1
- A single inductor on footprint #2
- Two parallel inductors
- An inductor on footprint #1 and a capacitor on footprint #2
- A capacitor on footprint #1 and an inductor on footprint #2

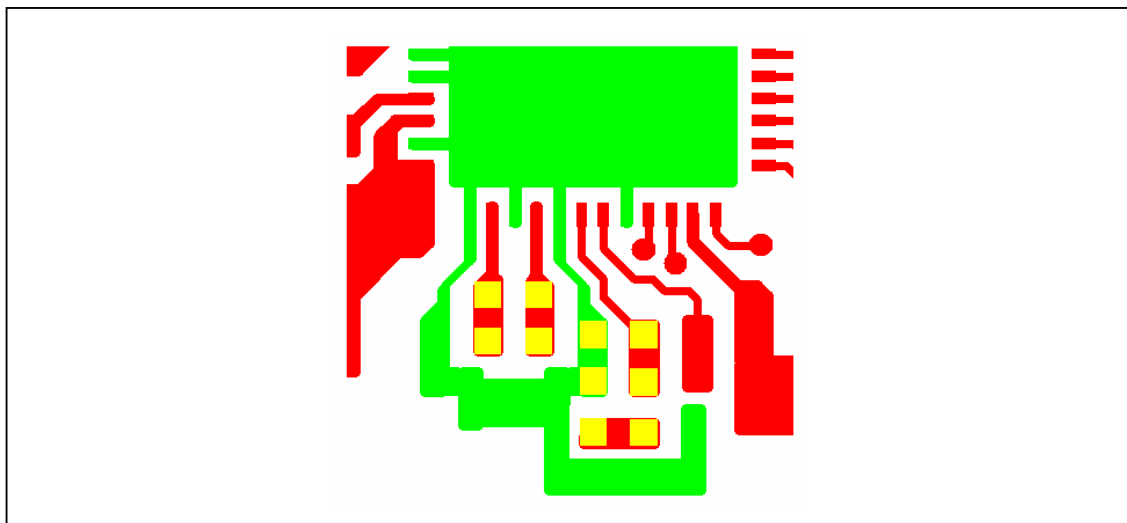
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To minimize the possibility of inductive cross coupling between the VCO and the transmitter and receiver blocks, it is recommended that the VCO inductor be placed orthogonal to the transmitter load inductor and the LNA balun inductor.



**Figure 8: VCO Tank Circuit Layout**

Similarly, the PLL loop filter circuit is illustrated below in Figure 9. Again, the PCB trace is kept as short as possible and the loop filter components are partially encased with a guard band. Care should be taken in this area as any noise that is injected into the loop filter will introduce noise (primarily FM noise) in the VCO itself.



**Figure 9: PLL Loop Filter**

### 4.2.2 Optimization

The VCO tank components should be determined so that the loop filter error voltage,  $V_{LFB}$ , is approximately 1.2 V at the band center frequency. This ensures that the both the VCO and PLL frequency synthesizer of the XE1200 series transceivers are functioning within their optimized operating regions, in terms of both VCO and phase detector gains.

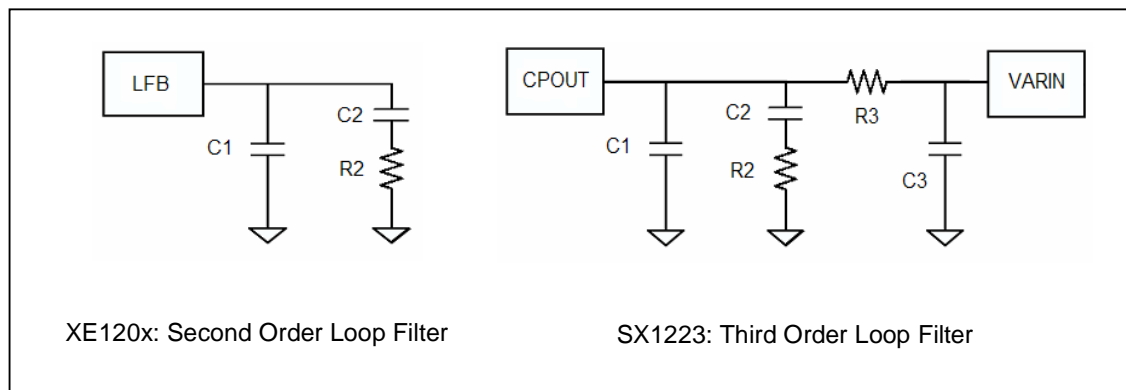
A high-Q wire wound inductor should be used to maximize VCO gain and minimize phase noise. However, if layout constraints mean that radiated emissions from the VCO are of major concern, then a 0402-size multilayer inductor should be fitted. Note however that multilayer inductors are not always symmetrical in terms of their radiation pattern and care should be taken when mounting during assembly.

If possible try to optimize the VCO without resorting to placing an external parallel capacitor to center the loop filter voltage. An external capacitor will degrade the Q of the tuned circuit. In addition, given the generally small value of capacitance required (typically less than 6.8pF) will be affected by the tolerance of the component. While it is possible to source small value capacitors with a tolerance of +/- 0.1pF, most commercially available parts have a tolerance of +/- 0.25pF. Since the gain of the VCO is in the region of 130 MHz/Volt, it can be seen tolerances in the order of greater than 10% could impact upon the operating region of the VCO and optimization of the PLL loop filter.

Note that Semtech's SX1223 transmitter IC incorporates an integrated VCO. As such software configuration register settings ensure that the VCO is operating within its optimum region.

To optimize the PLL loop filter it is recommended that the values quoted in Semtech's datasheets are a good starting point. The loop filter of the XE1200 series has an external second order loop filter (the third and higher order filter components are internal to the chip), while the SX1223 can be configured as either a second or third order loop filter, depending upon the device configuration.

An example of the loop filter configurations are illustrated below:



**Figure 10: Semtech Loop Filter Configurations**

Semtech have published a series of application notes and tools for optimizing the PLL loop filter circuit of both the XE1200 series and SX1223, and it recommended that these are reviewed should further optimization be required. Details can be found on the Semtech website at [www.semtech.com](http://www.semtech.com).

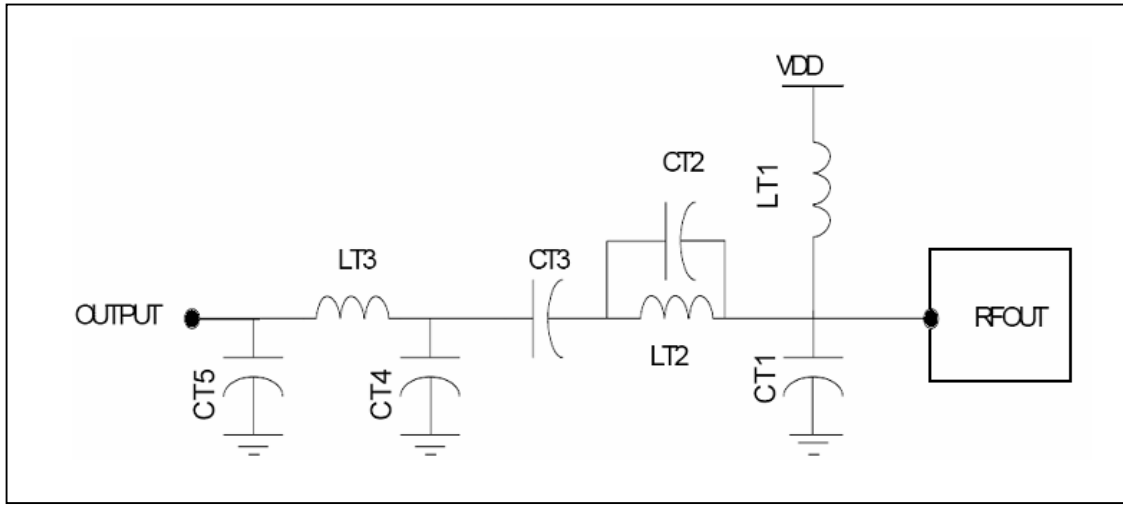
Use capacitors with a COG/NPO dielectric material in the loop filter since these offer low loss and stable electrical properties.

## 4.3 Transmitter Circuit

### 4.3.1 Optimization

The transmitter matching work serves two functions; firstly to present a tuned circuit load resonant at the desired output frequency, and secondly to attenuate the level of harmonic products generated due to circuit non-linearities.

Similar to the advice in Section 4.2.2, the data published in the Semtech datasheet is a good starting point for designing the transmitter matching network. This network is illustrated below in



**Figure 11: TX Matching Network**

The matching network is comprised of the following stages:

- LT1, CT1: Together with both PCB and device (packaging) parasitics forms a resonant load at the required output frequency.
- LT2, CT2: For applications that need to comply with the requirements of ETSI EN 300 220, this network forms a band stop filter resonant at the second harmonic.
- CT3 provides a DC block.
- CT4, CT5, LT3: Form a low-pass harmonic filter.

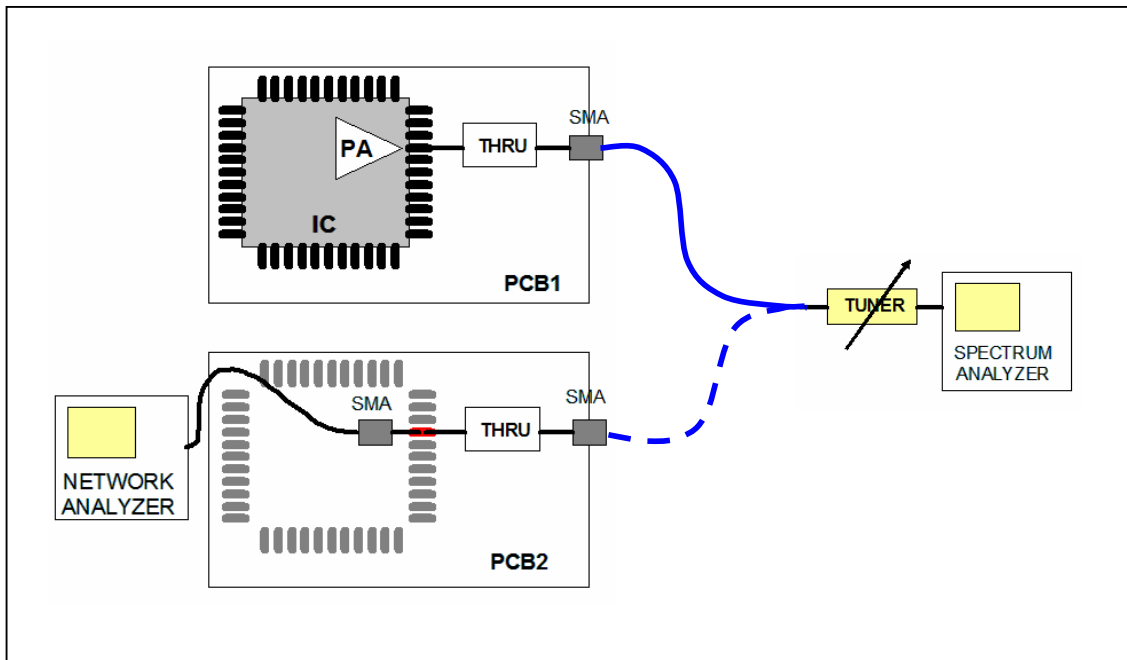
Note that these values were optimized on the Semtech reference design PCB and will probably not be the correct values for a new PCB layout. A method for implementing and optimizing the transmitter circuit on a new PCB layout is detailed below:

1. Populate two PCBs, one with the IC mounted (PCB1), the second with the IC removed (PCB2), but with the RFOUT pad open circuit. On PCB2 perform a one-port calibration of a vector network analyzer up to the RFOUT pad. While it is possible to purchase special mini-series RF connectors for this purpose, it is usually possible to connect to this pad with only minimal alteration to the surrounding pads and ground plane.
2. Ensure on both boards that a “thru” port exists from the RFOUT pad to the antenna port, by replacing all series components with a short-circuit and all shunt components with an open-circuit. The one exception is with the bias to the RFOUT port. Replace the inductor between the port and supply rail with a high-Q wirewound inductor, ensuring that at the supply rail this is well decoupled. This will provide a simple bias-T. The inductor value will typically depend upon the manufacturers’ type and specification. The inductor should present the highest impedance possible at the required test frequency, while operating below the self-resonant frequency of the device. From evaluation, a wirewound inductor of between 82nH and 120nH is suitable for 900 MHz. The test circuit is illustrated in Figure 12.
3. Connect the tuner or variable transmission line to the antenna port of PCB1. Configure the transmitter to the wanted output power mode and adjust the load presented by the tuner until

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the output power level displayed on the spectrum analyzer is the desired level. It is worth checking at the harmonic frequencies to verify that the load presented does not degrade the harmonic performance of the transmitter.

4. Now connect the tuner to PCB2 and note the reflection co-efficient presented at the RFOUT pad by this load impedance. This is the desired load that the transmitter needs to “see”. Note that the spectrum analyzer provides a 50 ohm termination for the tuner and should remain connected.
5. It is now possible to design the required network using a Smith Chart or design software.



**Figure 12: Measurement of Optimum Load Impedance Presented to the Transmitter**

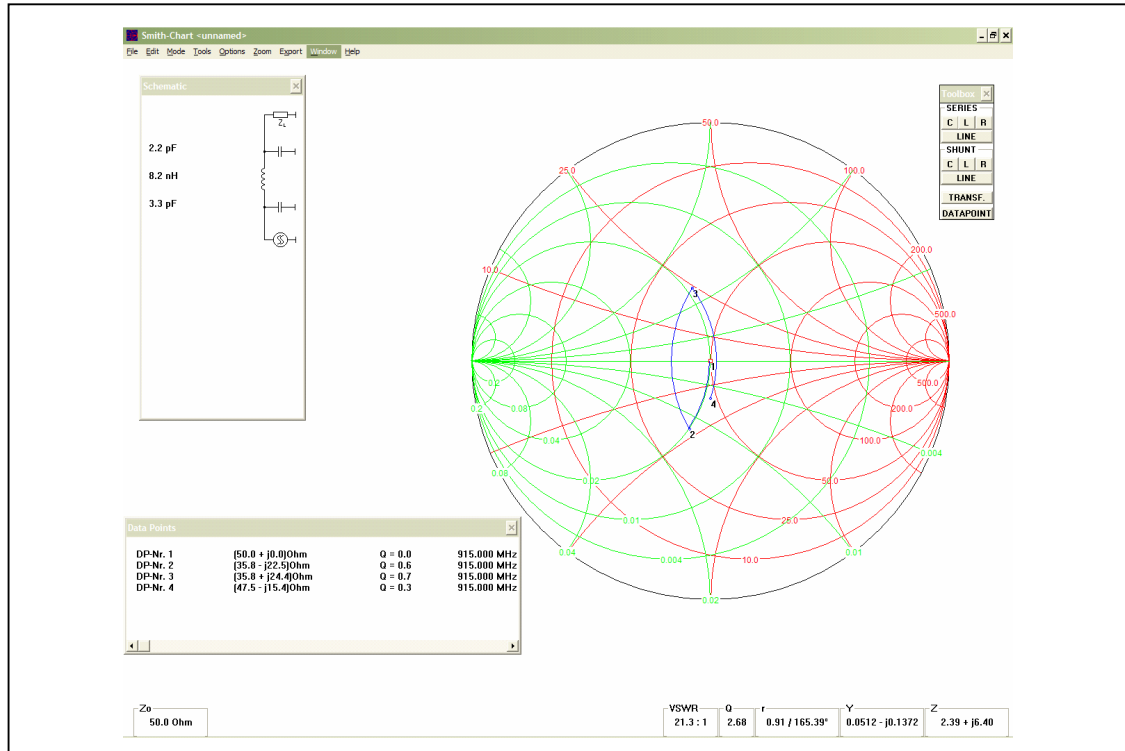
Alternatively, Semtech provides details of the optimum load impedance required to be presented to the transmitter output of their ISM band wireless ICs and these are summarized in Table 1 below:

Product	Mode	Frequency (MHz)		
		434	869	915
XE1203F	00 - 0 dBm	207 + j128	123 + j111	133 + j111
	01 - 5 dBm	172 + j84	125 + j95	133 + j103
	10 - 10 dBm	109 + j34	100 + j53	107 + j59
	<b>11 - 15 dBm</b>	<b>102 - j12</b>	<b>78 + j19</b>	<b>83 + j18</b>
XE1205	00 - 0 dBm	174 + j17	120 + j80	103 + j94
	01 - 5 dBm	117 + j22	115 + j79	101 + j77
	10 - 10 dBm	111 + j17	95 + j49	92 + j50
	<b>11 - 15 dBm</b>	<b>89 - j19</b>	<b>80 + j17</b>	<b>84 + j11</b>
SX1223	<b>111 - 10 dBm</b>	<b>20 - j3</b>	<b>24 - j1</b>	<b>24 + j8</b>

**Table 1: Optimum Transmitter Load Impedance**

A simple design procedure, using the XE1203F as an example is outlined below:

1. Starting at the antenna port or input to the RX/TX switch (which is assumed to be our 50 ohm reference point), design the pi-section harmonic trap and plot on the Smith Chart<sup>4</sup>, as represented in Figure 13, below.



**Figure 13: Design of Pi-Section Filter**

2. Add the series DC block and impedance transformation provided by the series inductor so that the impedance is transformed from nominally 50 ohms so that it lies on the same arc as the required load impedance, as illustrated in Figure 14.
3. Finally, design the tuned load to present the optimum impedance to be presented to the transmitter stage. From Figure 15, it can be observed that the overall Q of the matching network is less than 1.0.
4. The network can be implemented on stage by stage PCB2, enabling the engineer to check the theoretical results against those of the practical implementation.

<sup>4</sup> Smith V1.92: Berne Institute of Engineering and Architecture

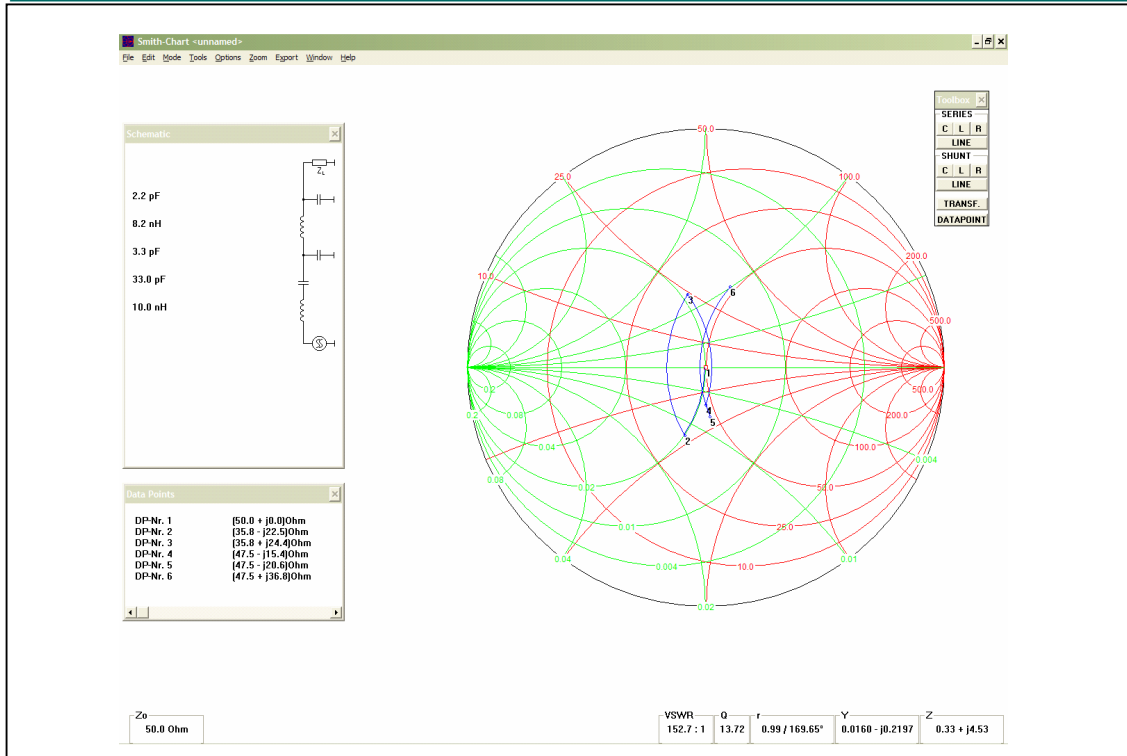


Figure 14: Impedance Transformation

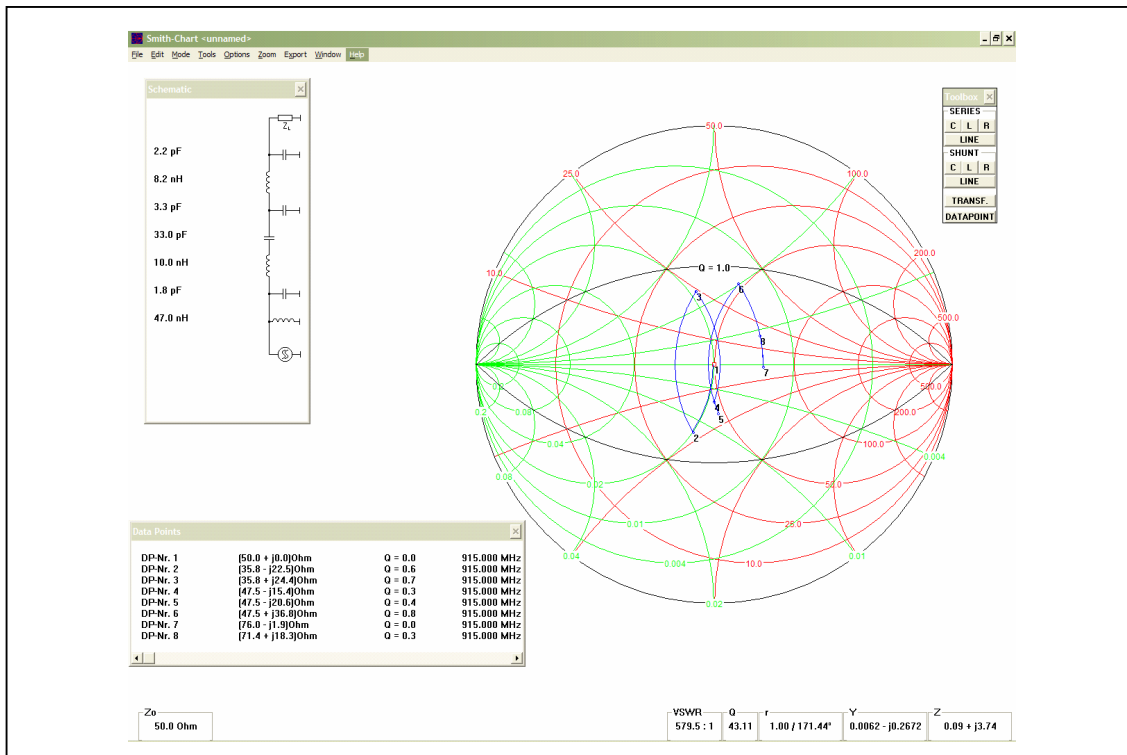


Figure 15: Optimized Matching Circuit

### 4.3.2 PCB Layout

The power supply to the transmitter section and the routing of the signal trace require careful consideration to eliminate not only potential current loops at RF frequencies but also to minimize the effects of inductive cross-coupling between different circuit blocks.



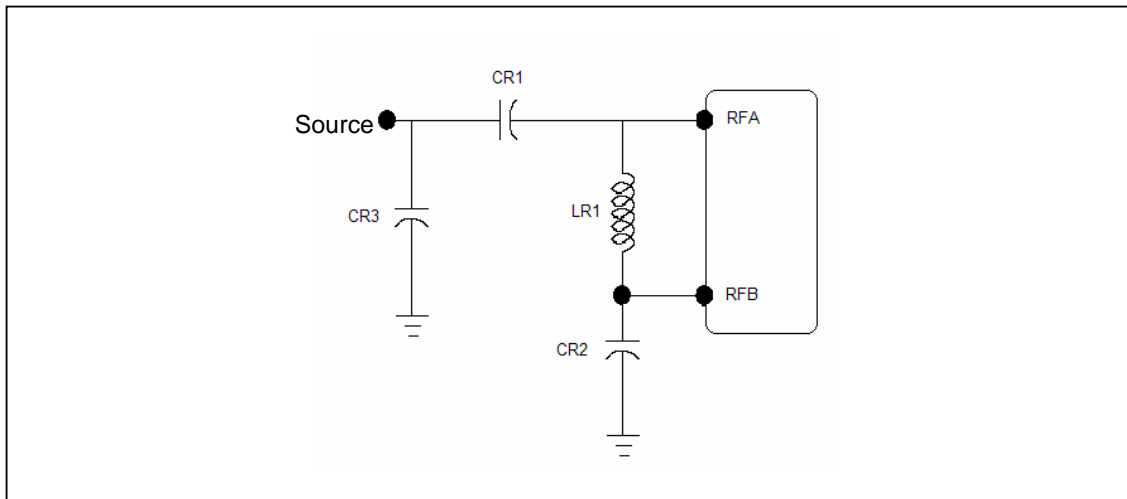
**Figure 16: Transmitter Section PCB Layout**

Figure 16 illustrates the PCB layout for the design calculated in Section 4.3.1. The power supply to both the transmitter (VDDP) and the RF block (VDDF) are decoupled by C21 and C2. The Load inductor, L2, is placed at right-angles to the VCO tank inductor (Section 4.2.1) and L1 to minimize inductive coupling. The circuit layout does not fold back upon itself so as again to minimize cross coupling.

## 4.4 Receiver LNA Circuit

### 4.4.1 PCB Layout

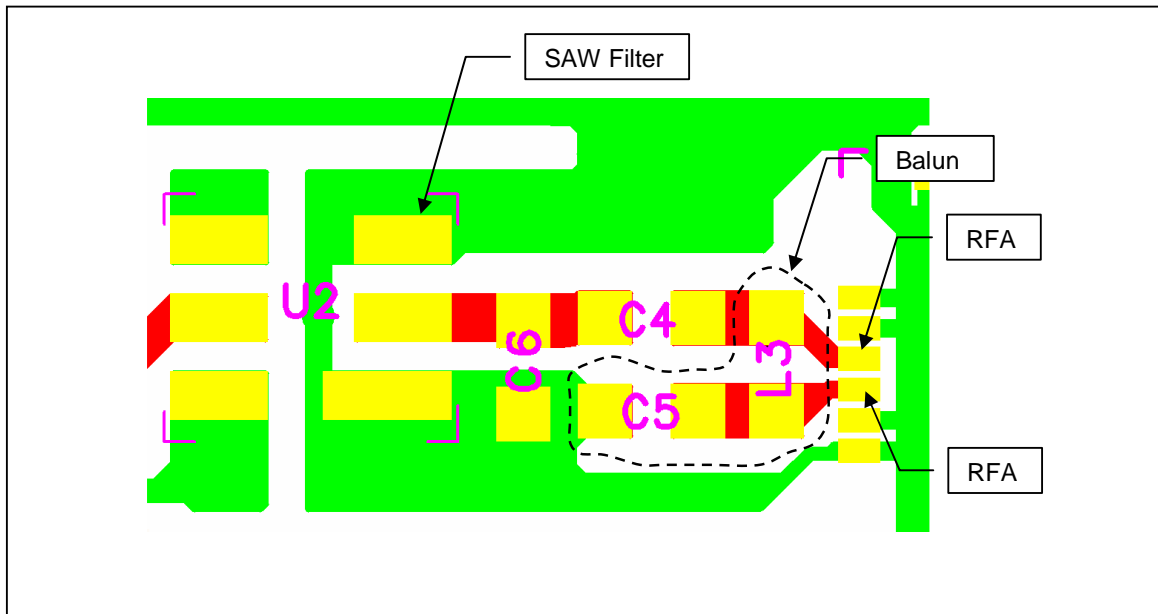
The schematic of the LNA matching network for the XE1200 series transceiver ICs is illustrated below in Figure 17:



**Figure 17: LNA Matching Network**

The network consists of a lumped element Balun, CR2 and LR1, to provide 180° phase shift to the differential input ports of the LNA at RFA and RFB. CR1 and CR3 (where required) to provide the impedance transformation and matching to the source impedance (nominally 50Ω).

Since the LNA provides a differential input, so the PCB layout should endeavor to respect the symmetry of this port as shown in Figure 18:



**Figure 18: LNA PCB Layout**

As can be seen above, the PCB layout of the lumped-element Balun (C5, L3) respects the symmetry of the differential LNA input (RFA, RFB). This example includes a SAW filter in the un-balanced path to the LNA which will greatly improve out-of-band blocking immunity of the receiver. C4 and C6 provide the impedance transformation so that the SAW filter is presented with a nominal 50Ω impedance.

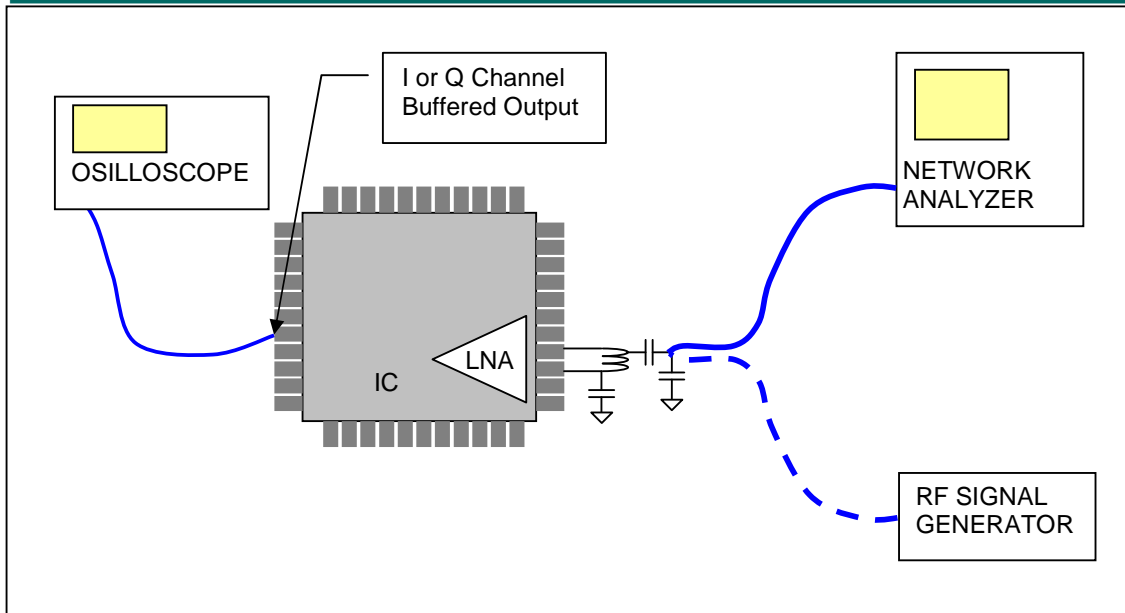
Semtech recommend that for most applications, provision be made for a SAW filter since ISM band devices share frequency spectrum with GSM/GPRS which operates close to the 863 - 870 MHz; and with fixed radio networks at when operating in the 902 - 928 MHz band.

#### 4.4.2 Circuit Optimization

The differential input impedance of the XE1200 TrueRF™ transceiver devices is approximately 6kΩ//0.5pF. While it would be possible to measure the differential port impedance with either a vector network analyzer capable of performing balanced port measurements, or by using a simple 4:1 voltage balun transformer (such as a  $\lambda/2$  transmission line type), when viewed on a Smith Chart the input impedance of the LNA will appear like an open circuit.

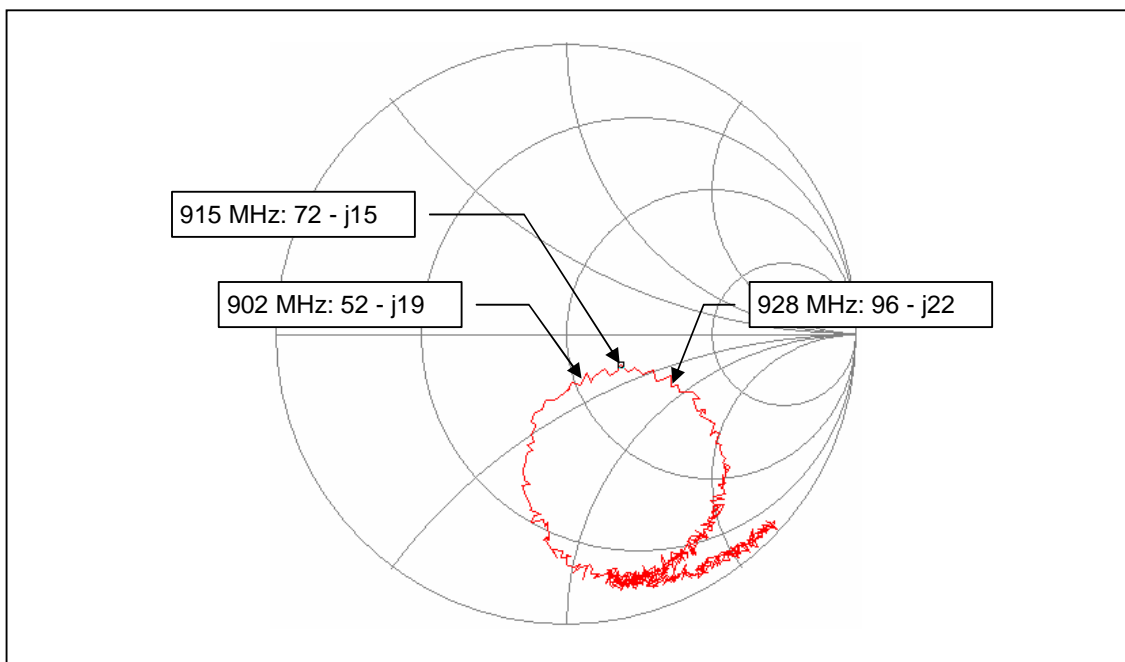
However, the recommended starting point is with the component values and circuit layout that is detailed in the Semtech datasheet and reference design for the transceiver, and then follow the simple optimization procedure below:

1. Connect the test circuit as illustrated in Figure 19. Note that the vector network analyzer reference plane should be connected to the junction of CR1 and CR3 in Figure 17, ensuring that the VNA power level does not overload the input to the receiver. Any components between this point and the antenna port should be replaced by an open-circuit.
2. Configure the transceiver in Receiver Mode and set the LNA to Mode A, select the required frequency band and baseband filter bandwidth by writing to the relevant configuration registers.



**Figure 19: Measurement and Optimization of the LNA Matching network**

3. Observe the impedance presented by the input reflection co-efficient,  $S_{11}$ , of the LNA input and matching network on the network analyzer. By component iteration, starting with the capacitors, modify the matching network so as the reflection coefficient at the band center frequency lies as close to the point of origin (or at least cuts the arc of constant reactance that passes through the origin). An example of a typical input match at 915 MHz is illustrated in Figure 20.



**Figure 20: Optimized LNA Matching Network Input Reflection Coefficient**

4. To verify that the LNA matching network is optimized, enable the I and Q channel buffered amplifiers by writing to the relevant configuration register. This allows the I and Q signals at the output of the baseband filters to be monitored on an oscilloscope.

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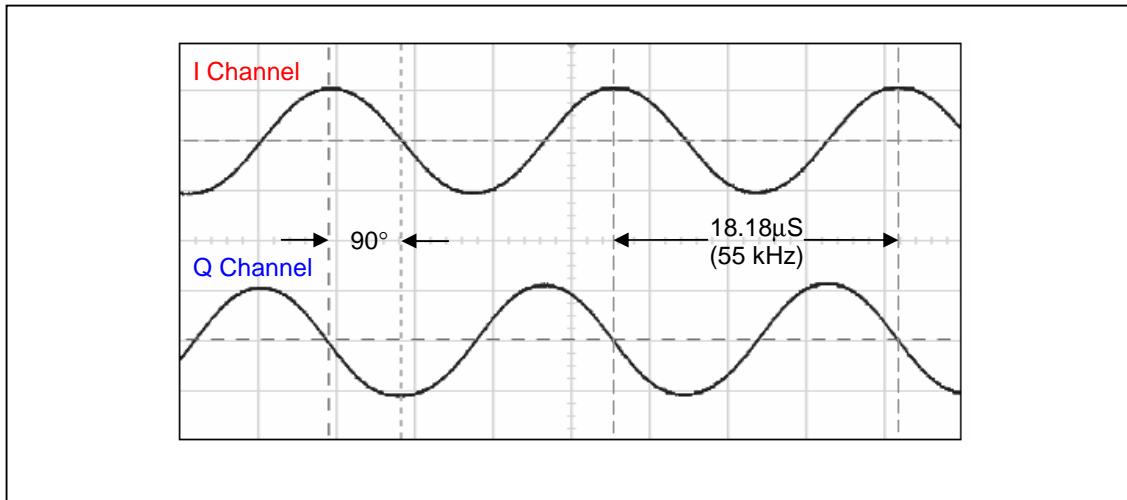
- Configure the RF signal generator to generate a 2-FSK signal and connect to the input of the optimized matching network. Ensure that the baseband filter bandwidth is set to accommodate dynamic single sideband bandwidth of the generated FSK signal. The dynamic bandwidth of the RF signal can be calculated as follows:

$$BW_{SSB} = \left( \frac{BR}{2} + f_{dev} \right) \tag{4.1}$$

- A table of typical peak-to-peak signal levels at the output of the I and Q buffered amplifiers as a function of the RF signal level incident at the input of the LNA matching network is tabulated below. By measuring both S11 and the I, Q channel signals it is possible to quickly verify that the optimum LNA matching network has been made. Figure 21 shows the I and Q channel signals for 4.8 kB signal modulated with a frequency deviation of 55 kHz. As can be seen, the frequency of the signal relates to the frequency deviation and not the data rate of the signal.

<i>RF Signal Level (dBm)</i>	<i>I, Q Channel Signal Level (mV<sub>pp</sub>)</i>
-50	2650
-60	2500
-70	1300
-80	500
-90	150
-95	90
-100	45
-105	30

**Table 2: Typical I, Q Signal Amplitudes**



**Figure 21: I and Q Channel Output Signals**

## 5 Passive Components

Just as the PCB and any active devices have associated parasitic elements, so do simple passive components such as capacitors and inductors. Knowledge of the physical properties of these passive components can assist with the circuit design and the choice of component.

### 5.1 Capacitors

From the illustration of the equivalent circuit of a capacitor, below, it can be seen that a capacitor has physical properties of both parasitic inductance,  $L_s$ , and resistance,  $R_s$ , associated with it. Typically these are shown as elements in series with the device capacitance. More complicated capacitance models include parallel parasitic capacitive and resistive elements<sup>5</sup>.

For RF applications it is generally recommended that multilayer (or monolithic) ceramic capacitors with a COG or NPO dielectric material, which is a highly stable Class I dielectric offering a linear temperature coefficient, low loss and stable electrical properties over time, voltage and frequency.

For RF decoupling purposes select a value of capacitor such that for the frequency to be decoupled is close to or just above the series resonant frequency (SRF) of the capacitor. At SRF the parasitic impedance resonates with the device capacitance to form a series tuned circuit and the impedance presented by the capacitor is the effective series resistance (ESR), represented by  $R_s$ .

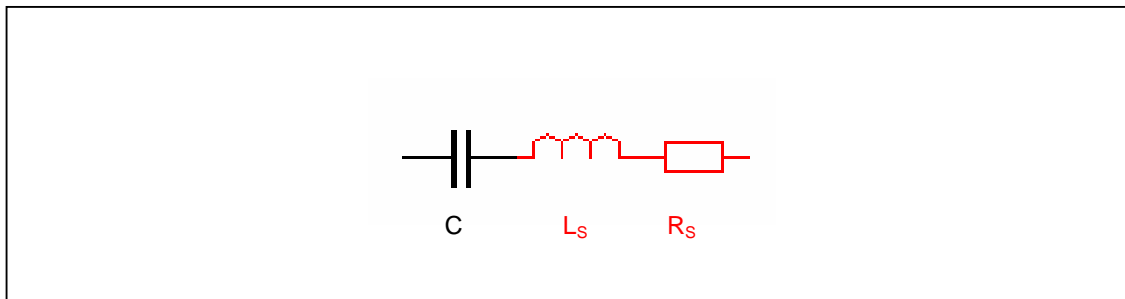
As has been noted above, capacitors also have associated parallel parasitic components, giving rise to a parallel resonant frequency (PRF), whereby the capacitor behaves like a parallel tuned circuit and presents a high impedance to the circuit. As a rule of thumb, the PRF is approximately twice the SRF.

Always use the appropriate decoupling capacitance in the circuit design. Typical decoupling capacitor values for the various frequency blocks of Semtech ISM band wireless ICs are tabulated below:

<b>Decoupling Circuit</b>	<b>Capacitor Type</b>
RF Stages: 869 MHz - 915 MHz	33pF - 68pF; COG/NPO Dielectric material
RF Stages: 434 MHz	82pF - 150pF; COG/NPO Dielectric material
39 MHz Reference Oscillator	1nF - 4.7nF; COG/NPO or X7R Dielectric material
Digital/Low Frequency Blocks	Up to 1 $\mu$ F; X7R or Y5V Dielectric Material

**Table 3: Typical Decoupling Capacitor Values**

For DC blocking or coupling applications at RF, typically a capacitor with low insertion loss and a good quality or Q-factor is required. Since a capacitor's Q-factor is inversely proportional to its ESR, select a capacitor with a low ESR and ensure that the SRF of the capacitor is greater than the frequency of operation. If the frequency is above the SRF of the capacitor, the capacitor will appear inductive and will behave as a "DC blocking inductor". Since the value of the coupling capacitor will be in the pF range, select a type with COG/NPO dielectric.

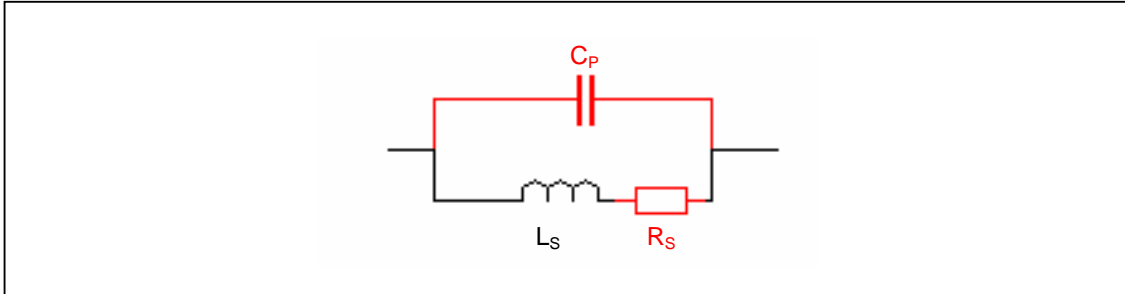


**Figure 22: Equivalent Circuit of a Multilayer Ceramic Capacitor**

<sup>5</sup> "SRF and PRF and their relationship to RF Capacitor Applications", Johanson Technology

## 5.2 Inductors

Just as a capacitor has parasitic resistance and inductance associated with it, so an inductor has parasitic elements associated with it, as illustrated below:



**Figure 23: Inductor Equivalent Circuit**

$C_P$  is normally considered to be the inter-winding capacitance that exists between the turns of the inductor (either a wirewound or multi-layer type). However, if the inductor is placed over a ground plane then this capacitance will also include the capacitance that exists between the inductor and the ground plane.  $R_S$  can be considered as the resistance of the inductor winding.

In terms of circuit performance, the self-resonant frequency and Q-factor are important inductor parameters that should be taken into consideration, especially for high-Q circuits, such as the LNA matching network or where circuit losses need to be minimized, such as with transmitter circuit. For the VCO tank inductor a high-Q component will reduce VCO phase noise (while a 0402 component will minimize the radiation pattern).

At the self-resonant frequency, the impedance of the inductor is at a maximum. However, since the capacitive reactance cancels with the inductive reactance, both the net inductance and Q are at a minimum.

From the above it can be seen that the SRF of the inductor should be higher than the frequency of the circuit in which the inductor is operating.

In general wirewound inductors have a higher Q-factor than a multilayer equivalent. However, they will also reflect and radiate more energy which can give rise to higher emission levels, especially in terms of self-coupling of the local oscillator into the LNA. Generally, wirewound and multilayer types are not interchangeable without some variation in circuit performance.

As has been noted, inductive coupling can give rise to unforeseen (and undesired) circuit operation. To minimize coupling, mount inductors in sensitive circuit areas at 90 degrees to one another.

While there is a move towards symmetrical windings for inductors, multi-layer types which are wound horizontally normally have an identification mark indicating the start or stop of the winding (it can vary from manufacturer to manufacturer). It is recommended that non-symmetrical inductors be orientated in the same direction during the manufacturing.

Table 4 below outlines typical inductor component types that have been employed to ensure successful RF designs.

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<i>Circuit Block</i>	<i>Inductor Type</i>
VCO	Wirewound 0402-size for minimum VCO phase noise
	Multilayer 0603-size
LNA Balun	Wirewound for optimum RX sensitivity
	Multilayer to minimize LO self-reception
Transmitter Circuit	Multilayer 0603-size

**Table 4: Typical Inductor Types**

From experience and for applications in the ISM bands, Semtech do not specify a particular capacitor vendor or part number on our reference design Bill-of-Material. However, for inductor values and type Semtech recommend that the same inductor type from a particular vendor is used in both development and manufacture.

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