

Description

The ACS8530 is a highly integrated, single-chip solution for the Synchronous Equipment Timing Source (SETS) function in a SONET or SDH Network Element. The device generates SONET or SDH Equipment Clocks (SEC) and Frame Synchronization clocks. The ACS8530 is fully compliant with the required international specifications and standards.

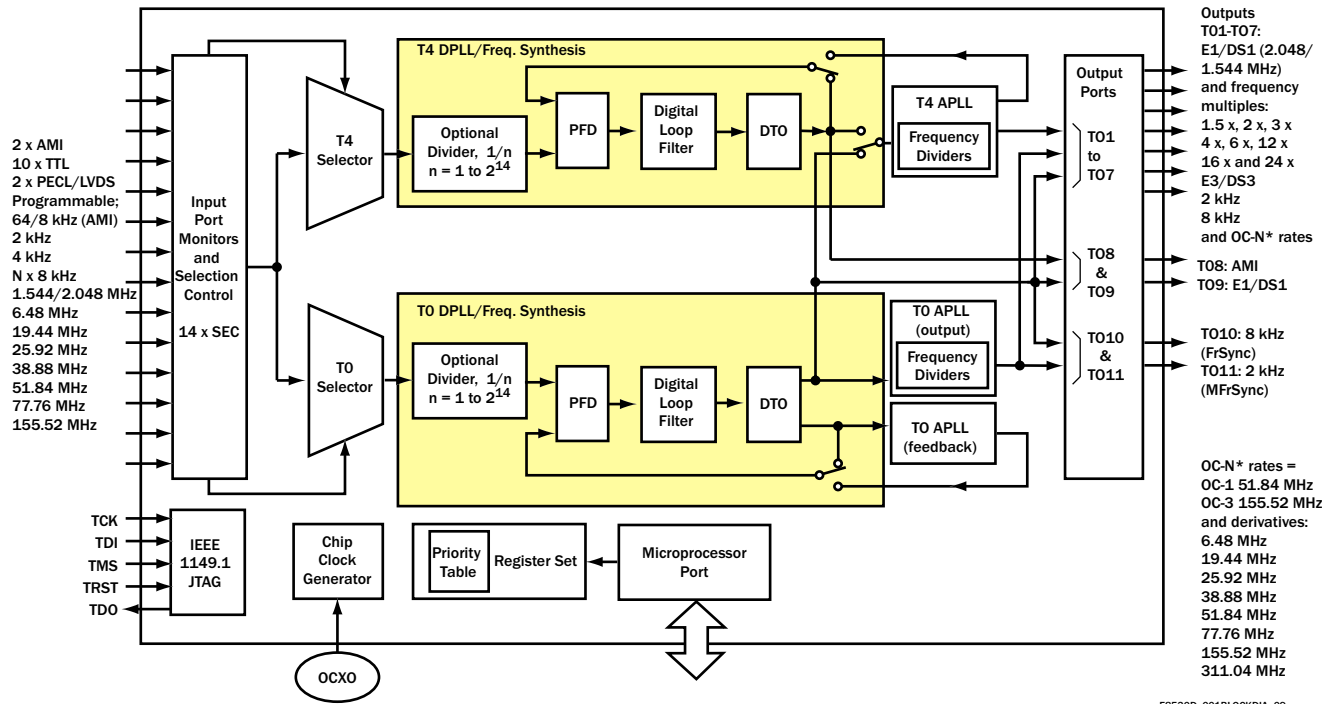
The device supports Free-run, Locked and Holdover modes. It also supports all three types of reference clock source: recovered line clock, PDH network, and node synchronization. The ACS8530 generates independent SEC and BITS clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

Two ACS8530 devices can be used together in a Master/Slave configuration mode allowing system protection against a single ACS8530 failure.

A microprocessor port is incorporated, providing access to the configuration and status registers for device setup and monitoring. The ACS8530 supports IEEE 1149.1 JTAG boundary scan.

Block Diagram

Figure 1 Block Diagram of the ACS8530 SETS



Pin Diagram

Figure 2 ACS8530 Pin Diagram

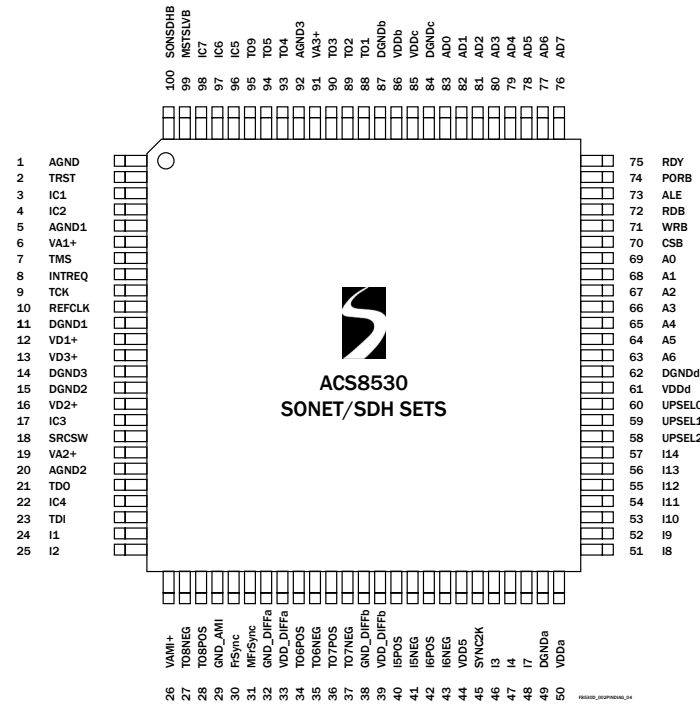


Table 1 Power Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
11, 14, 15,	DGND1, DGND3, DGND2,	P	-	Supply Ground: Digital ground for components in PLLs.
49, 62, 84, 87	DGNDa, DGNDd, DGNDc, DGNDb	P	-	Supply Ground: Digital ground for logic.
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output.
32, 38	GND_DIFFa, GND_DIFFb	P	-	Supply Ground: Digital ground for differential ports.
1, 5, 20, 92	AGND, AGND1, AGND2, AGND3	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected

Pin No.	Symbol	I/O	Type	Description
3, 4, 17, 22, 96, 97, 98	IC1, IC2, IC3, IC4, IC5, IC6, IC7	-	-	Internally Connected: Leave to Float.

Pin Description

Table 1 Power Pins

Pin No.	Symbol	I/O	Type	Description
12, 13, 16	VD1+, VD3+, VD2+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
26	VAMI+	P	-	Supply Voltage: Digital supply to AMI output, +3.3 Volts ±10%.
33, 39	VDD_DIFFa, VDD_DIFFb	P	-	Supply Voltage: Digital supply for differential ports, +3.3 Volts ±10%.
44	VDD5	P	-	Digital Supply for +5 Volts Tolerance to Input Pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86	VDDa, VDDd, VDDc, VDDb	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
6	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
19, 91	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs, +3.3 Volts ±10%.

Table 3 Other Pins

Pin No.	Symbol	I/O	Type	Description
2	TRST	I	TTL _D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for Boundary Scan stand-by mode, still allowing correct device operation. If not used connect to GND or leave floating.
7	TMS	I	TTL ^U	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL/CMOS	Interrupt Request: Active High/Low software Interrupt output.
9	TCK	I	TTL _D	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating.
10	REFCLK	I	TTL	Reference Clock: 12.800 MHz
18	SRC5W	I	TTL _D	Source Switching: Force Fast Source Switching.
21	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL ^U	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.

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Table 3 Other Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
24	I1	I	AMI	Input Reference 1: Composite clock 64 kHz + 8 kHz.
25	I2	I	AMI	Input Reference 2: Composite clock 64 kHz + 8 kHz.
27	TO8NEG	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz negative pulse.
28	TO8POS	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz positive pulse.
30	FrSync	O	TTL/CMOS	Output Reference 10: 8 kHz Frame Sync output.
31	MFrSync	O	TTL/CMOS	Output Reference 11: 2 kHz Multi-Frame Sync output.
34, 35	TO6POS, TO6NEG	O	LVDS/PECL	Output Reference 6: Programmable, default 38.88 MHz, default type LVDS.
36, 37	TO7POS, TO7NEG	O	PECL/LVDS	Output Reference 7: Programmable, default 19.44 MHz, default type PECL.
40, 41	I5POS, I5NEG	I	LVDS/PECL	Input Reference 5: Programmable, default 19.44 MHz, default type LVDS.
42, 43	I6POS, I6NEG	I	PECL/LVDS	Input Reference 6: Programmable, default 19.44 MHz, default type PECL.
45	SYNC2K	I	TTL _D	External Sync input: 2 kHz, 4 kHz or 8 kHz for frame alignment.
46	I3	I	TTL _D	Input Reference 3: Programmable, default 8 kHz.
47	I4	I	TTL _D	Input Reference 4: Programmable, default 8 kHz.
48	I7	I	TTL _D	Input Reference 7: Programmable, default 19.44 MHz.
51	I8	I	TTL _D	Input Reference 8: Programmable, default 19.44 MHz.
52	I9	I	TTL _D	Input Reference 9: Programmable, default 19.44 MHz.
53	I10	I	TTL _D	Input Reference 10: Programmable, default 19.44 MHz.
54	I11	I	TTL _D	Input Reference 11: Programmable, default (Master mode) 1.544/2.048 MHz, default (Slave mode) 6.48 MHz.
55	I12	I	TTL _D	Input Reference 12: Programmable, default 1.544/2.048 MHz.
56	I13	I	TTL _D	Input Reference 13: Programmable, default 1.544/2.048 MHz.
57	I14	I	TTL _D	Input Reference 14: Programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL _D	Microprocessor select: Configures the interface for a particular microprocessor type at reset.

Table 3 Other Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
63 - 69	A(6:0)	I	TTL _D	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode - output in EPROM mode only.
70	CSB	I	TTL ^U	Chip Select (Active Low): This pin is asserted Low by the microprocessor to enable the microprocessor interface - output in EPROM mode only.
71	WRB	I	TTL ^U	Write (Active Low): This pin is asserted Low by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL ^U	Read (Active Low): This pin is asserted Low by the microprocessor to initiate a read cycle.
73	ALE	I	TTL _D	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from High to Low, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL ^U	Power-On Reset: Master reset. If PORB is forced Low, all internal states are reset back to default values.
75	RDY	O	TTL/CMOS	Ready/Data Acknowledge: This pin is asserted High to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	I/O	TTL _D	Address/Data: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.
88	TO1	O	TTL/CMOS	Output Reference 1: Programmable, default 6.48 MHz.
89	TO2	O	TTL/CMOS	Output Reference 2: Programmable, default 38.88 MHz.
90	TO3	O	TTL/CMOS	Output Reference 3: Programmable, default 19.44 MHz.
93	TO4	O	TTL/CMOS	Output Reference 4: Programmable, default 38.88 MHz.
94	TO5	O	TTL/CMOS	Output Reference 5: Programmable, default 77.76 MHz.
95	TO9	O	TTL/CMOS	Output Reference 9: 1.544/2.048 MHz, as per ITU G.783 BITS requirements.
99	MSTSLVB	I	TTL ^U	Master/Slave Select: sets the state of the Master/Slave selection register, Reg. 34, Bit 1.
100	SONSDHB	I	TTL _D	SONET or SDH Frequency Select: sets the initial power up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4. When set Low, SDH rates are selected (2.048 MHz etc.) and when set High, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

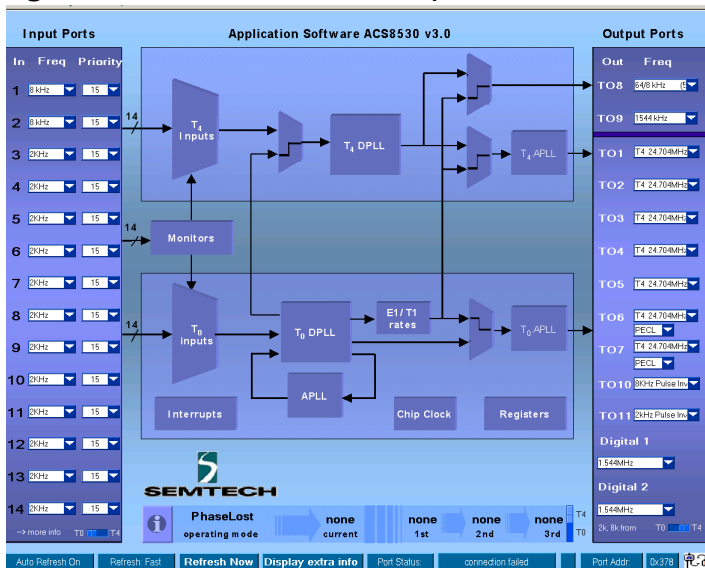
The ACS8530 SETS device is the industry standard single-chip solution for all of the SETS functions in both SONET and SDH Network Elements. It is a highly integrated and easily configurable device which generates and maintains accurate and stable SEC and Frame/Multi-Frame Synchronization pulse outputs, compliant with the required international telecom specifications and standards. The ACS8530 provides a simple, compact, highly flexible synchronization solution, which can be easily tailored for use with a range of transmission formats and rates, via software configuration.

The ACS8530 employs various mechanisms to maintain the integrity of its output clocks when its input clocks fail or fall below the required specification levels. By smoothing out the effects of these input anomalies, the ACS8530 improves the overall stability and reliability of the downstream system synchronization, which translates to improved quality of service.

In addition to the benefits of having all the SETS functionality on one chip, a key architectural advantage that the ACS8530 has over traditional solutions is in the use of Digital Phase Locked Loop (DPLL) technology for precise and repeatable performance over temperature or voltage variations and between parts.

Semtech can provide an Evaluation Board and an intuitive, GUI-based Software package so that designers can rapidly appraise the ACS8530 SETS device and see for themselves the benefits that a Semtech SETS solution can bring to their designs.

Figure 3 Evaluation Software Graphical User Interface



General Description

Inputs

The ACS8530 SETS device accepts 14 input clocks via the input ports (10 x TTL, 2 x PECL/LVDS, 2 x AMI). All the TTL/CMOS ports are 3 V and 5 V compatible (with clamping if required by connecting the VDD5 pin). The AMI inputs are typically ± 1 V A.C. coupled.

Input frequencies supported range from 2 kHz to 155.52 MHz. Common E1, DS1, OC-3 and sub-divisions are supported as spot frequencies to which the DPLLs will directly lock.

Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via a built-in programmable divider. The ACS8530 supports all three types of reference clock source: Recovered Line Clock, PDH Network Synchronization Timing and Node Synchronization. Refer to Table 4 for details of each input port.

Monitors

A monitoring function constantly appraises the frequency/activity of each input reference source, and reports anomalous behavior. Each of the 14 input monitors is individually configurable, allowing flags or interrupts to be raised which can influence both the operating state of the device and which inputs are available for selection by the PLL circuitry. Any reference source which suffers a loss-of-activity or clock-out-of-band condition will be declared as unavailable.

Anomalies detected by the activity detector are integrated in a Leaky Bucket Accumulator. Occasional anomalies do not cause the Accumulator to cross the alarm setting threshold, so the selected reference source is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected reference source being rejected.

The ACS8530 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range measured with respect either to the output clock or to the XO clock. A soft alarm is raised if the drift is outside ± 11.43 ppm and a hard alarm is raised if the drift is outside ± 15.24 ppm.

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- Fast detection on input failure and entry into Holdover mode (holds at the last good frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks

T0 Additional Features:

- Non-revertive mode
- Phase Build-out (PBO) on source switch (hit-less source switching)
- PBO following phase hit on locked-to source
- I/O phase offset control
- Greater programmable bandwidth from 0.5 MHz to 70 Hz in 18 steps (T4 path programmable bandwidth in 3 steps, 18, 35 and 70 Hz)
- Noise rejection on low frequency inputs
- Manual Holdover frequency control
- Controllable automatic Holdover frequency filtering
- Frame Sync pulse alignment

Either the software or an internal state machine controls the operation of the DPLL in the T0 path. The state machine for the T4 path is very simple and cannot be manually/externally controlled, however the overall operation can be controlled by using manual reference source selection. The T4 path can be used to measure phase difference between two inputs.

The T0 path DPLL always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins. The T4 path can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. When the T4 path is selected to lock to the T0 path, the T4 DPLL locks to 8 kHz supplied from the T0 DPLL. This is because all of the frequencies of operation of the T4 path can be divided to 8 kHz and this ensures synchronization of all the frequencies (except 2 kHz) within the two paths.

Outputs

The PLLs work together to ensure a number of frequencies are simultaneously available for selection at the 11 output ports (8 x TTL, 2 x PECL/LVDS, 1 x AMI).

The various configurations make the ACS8530 capable of generating a total of 55 possible output frequencies.

The ACS8530 can be configured to support OC-N, E1/DS1, E3/DS3 and BITS outputs, together with an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock. Tables 5 and 6 summarize the output frequency/jitter options and technologies supported for each output port.

Table 5 Output Port Frequencies and Technologies

Port Name	Output Port Technology	Frequencies Supported
T01	TTL/CMOS	See Table 6
T02	TTL/CMOS	
T03	TTL/CMOS	
T04	TTL/CMOS	
T05	TTL/CMOS	
T06	LVDS/PECL (LVDS default)	
T07	PECL/LVDS (PECL default)	
T08	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz), fixed frequency.
T09	TTL/CMOS	Either 1.544 MHz or 2.048 MHz.
T010	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7C.
T011	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7C.

Table 6 T01 to T07 Frequency/Jitter Options

Frequency (MHz)	Jitter Level (typ)	
	rms (ps)	pk-pk (ns)
2 kHz	60	0.6
8 kHz	60	0.6
1.536 (not T04/T05)	250	1.5
1.544 (not T04/T05)	150	1.0
2.048	220	1.2
2.0586667	150	1.0
2.316 (not T04/T05)	110	0.75
2.7306667	220	1.2
2.796 (not T04/T05)	110	1.0
3.088	110	0.75
3.728	110	1.0
4.096 via Digital1 (not T07) or Digital2 (not T06)	3800	13
4.296 (not T04/T05)	120	1.0
4.86 (not T04/T05)	60	0.6
5.728	120	1.0
6.144	250	1.5
6.176	150	1.0
6.48	60	0.6
8.192	220	1.2
8.2346667	760	2.6
9.264	110	0.75
10.922667	250	1.6
11.184	110	1.0
12.288	250	1.5
12.352	110	0.75
16.384	220	1.2
16.46933	760	2.6
17.184	120	1.0

Table 6 T01 to T07 Frequency/Jitter Options (cont...)

Frequency (MHz)	Jitter Level (typ)	
	rms (ps)	pk-pk (ns)
18.528	110	0.75
19.44	60	0.6
21.84533	250	1.6
22.368	110	1.0
24.576	250	1.5
24.704	110	0.75
25.92	60	0.6
32.768	220	1.2
34.368	120	1.0
37.056	110	0.75
38.88	60	0.6
44.736	110	1.0
49.152 (T04/T05 only)	250	1.5
49.152 (T06/T07 only)	900	4.5
49.408 (T04/T05 only)	150	1.0
49.408 (T06/T07 only)	760	2.6
51.84	60	0.6
65.536 (T04/T05 only)	220	1.2
65.536 (T06/T07 only)	120	1.0
68.736	120	1.0
74.112 (T04/T05 only)	110	0.75
74.112 (T06/T07 only)	110	0.75
77.76	60	0.6
89.472 (T04/T05 only)	110	1.0
98.304 (T06 only)	900	4.5
98.816 (T06 only)	760	2.6
131.072 (T06 only)	250	1.6
137.472 (T04/T05 only)	120	1.0
148.224 (T06 only)	110	0.75
155.52	60	0.6
311.04 (T06 only)	60	0.6

Modes of Operation

The device has three principle modes of operation: Free-run, Locked, and Holdover. In Free-run mode, the ACS8530 is not synchronized to an input reference source. It generates a stable, low-noise clock signal derived from, and with the same frequency accuracy as, the external oscillator. The accuracy can be enhanced via software calibration to within ± 0.0196229 ppm.

In Locked mode, the ACS8530 selects the most appropriate input reference source from its 14 available inputs and generates a stable, low-noise clock signal locked to the selected reference. When the Locked mode is achieved, the output signal is phase locked to the selected input reference source. The selected input reference source is determined by the priority table.

When the ACS8530 is in Locked mode, the output frequency and phase follows that of the selected input reference source.

In Holdover mode, the ACS8530 generates a stable, low-noise clock signal from the internal oscillator, adjusted to match the last known good frequency of the last selected reference source. The device uses stored data, acquired when the input reference source was still valid, to control its output frequency. The ACS8530 provides several configurable modes for refining Holdover operation.

Input Selection Priorities

Each input reference can be programmed with a priority number (see Table 4) allowing references to be chosen according to the highest priority valid input. The two paths (T0 and T4) have their own separate priority settings so that the paths can operate independently. Both paths operate either automatic or external source selection. Table 4 gives details of the input reference ports. Specific frequencies and priorities are set by configuration.

Automatic Selection

Under normal operation, the input reference sources are selected automatically by an order of priority. But, for special circumstances such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects a reference source based on its predefined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially defined by the default configuration and can be changed, via the microprocessor interface, by the Network Manager. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, then the next-highest source is selected.

Ultra Fast Switching

Reference sources are monitored using a Leaky Bucket approach to allow source qualification criterion to be monitored. A reference source is normally disqualified after the Leaky Bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented so that a loss of activity of just a few reference clock cycles will raise an alarm and cause a reference switch.

External Protection Switching

External Switching mode, for fast switching between inputs I3 or I5 and I4 or I6, can also be triggered directly from a dedicated pin (SRCSW).

Performance

Conformance

In all modes of Operation, the frequency accuracy, jitter and drift performance of the clocks meet the requirements of the following specifications:

ITU-T: G.736, G.742, G783, G.812, G.813, G.822, G.823, G.824, G.825.

Telcordia: GR-253-CORE, Issue 3; GR-499-CORE, Issue 2; GR-1244-CORE, Issue 2.

ANSI: T1.101-1999.

ETSI: ETS 300 462-3, ETS 300 462-5.

Performance Benefits from DPLL/APLL Technology

The use of Digital Phase Locked Loop technology ensures precise and repeatable performance over temperature or voltage variations, and between parts. The overall PLL bandwidth, loop damping, pull-in range and frequency accuracy are all determined by digital parameters that provides a consistent level of performance. An APLL takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of

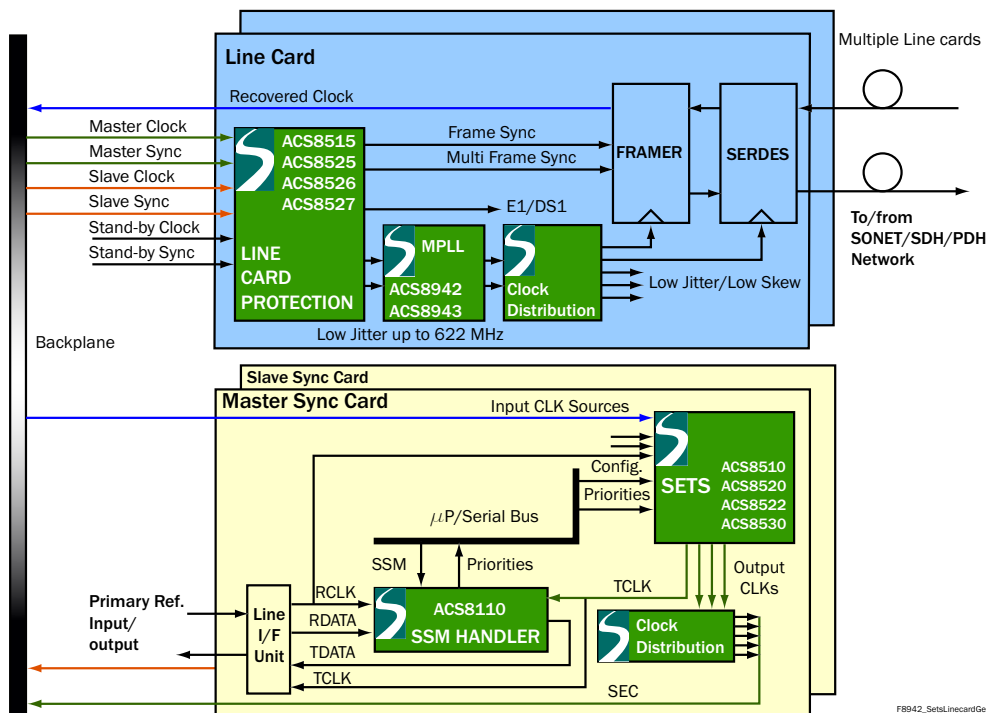
magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach.

The DPLLs are clocked by the external oscillator module (OCXO) therefore the Free-run or Holdover frequency stability is only determined by the stability of the external oscillator module. This second key advantage confines all temperature critical components to one well defined and pre-calibrated module, whose performance can be chosen to match the application; for example, an OCXO for Stratum 3E applications.

All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range, for example, can all be set directly. The PLL bandwidth can be set over a wide range, 0.5 mHz to 70 Hz in 18 steps, to cover all SONET/SDH clock synchronization applications. A high level of phase and frequency accuracy is made possible in the ACS8530 by an internal resolution of up to 54 bits and internal Holdover accuracy up to 7.5×10^{-14} (instantaneous).

Typical Application

Figure 4 Semtech's Product Family Solution for a Typical SONET/SDH Architecture



F8942_SetsLineCardGenApp_02

Register Map
Table 7 Register Map

Register Name	Address (hex)	Default (hex)	Data Bit								
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
RO = Read Only R/W = Read/Write											
chip_id (RO)	00	52	Device part number [7:0] 8 least significant bits of the chip ID								
	01	21	Device part number [15:8] 8 most significant bits of the chip ID								
chip_revision (RO)	02	00	Chip revision number [7:0]								
test_register1 (R/W)	03	14	phase_alarm	disable_180		resync_analog	Set to zero	8K edge polarity	Set to zero	Set to zero	
sts_interrupts (R/W)	05	FF	I8 valid change	I7 valid change	I6 valid change	I5 valid change	I4 valid change	I3 valid change	I2 valid change	I1 valid change	
	06	3F	operating_mode	main_ref_failed	I14 valid change	I13 valid change	I12 valid change	I11 valid change	I10 valid change	I9 valid change	
sts_current_DPLL_frequency, see OC/OD	07	00						Bits [18:16] of current DPLL frequency			
sts_interrupts (R/W)	08	50	Sync_ip_alarm	T4_status	phasemon_alarm	T4_inputs_failed	AMI2_Viol	AMI2_LOS	AMI1_Viol	AMI1_LOS	
sts_operating (RO)	09	41	SYNC2K_alarm	T4_DPLL_lock	TO_DPLL_freq_soft_alarm	T4_DPLL_freq_soft_alarm	TO_DPLL_operating_mode				
sts_priority_table (RO)	0A	00	Highest priority validated source				Currently selected source				
	0B	00	3rd highest priority validated source				2nd highest priority validated source				
sts_current_DPLL_frequency [7:0] (RO)	0C	00	Bits [7:0] of current DPLL frequency								
	0D	00	Bits [15:8] of current DPLL frequency								
	07	00	Bits [18:16] of current DPLL offset								
sts_sources_valid (RO)	0E	00	I8	I7	I6	I5	I4	I3	I2	I1	
	0F	00			I14	I13	I12	I11	I10	I9	
sts_reference_sources (RO)			Out-of-band alarm (soft)	Out-of-band alarm (hard)	No Activity alarm	Phase lock alarm	Out-of-band alarm (soft)	Out-of-band alarm (hard)	No activity alarm	Phase lock alarm	
Status of Input pairs (1 & 2) (3 & 4) (5 & 6) (7 & 8) (9 & 10) (11 & 12) (13 & 14)	10	66	Status of I2 Input				Status of I1 Input				
	11	66	Status of I4 Input				Status of I3 Input				
	12	66	Status of I6 Input				Status of I5 Input				
	13	66	Status of I8 Input				Status of I7 Input				
	14	66	Status of I10 Input				Status of I9 Input				
	15	66	Status of I12 Input				Status of I11 Input				
	16	66	Status of I14 Input				Status of I13 Input				
cnfg_ref_selection_priority (1 & 2) (R/W)	18	32	programmed_priority I2				programmed_priority I1				
	19	54	programmed_priority I4				programmed_priority I3				
	1A	76	programmed_priority I6				programmed_priority I5				
	1B	98	programmed_priority I8				programmed_priority I7				
	1C	BA	programmed_priority I10				programmed_priority I9				
	1D	DC	programmed_priority I12				programmed_priority I11				
	1E	FE	programmed_priority I14				programmed_priority I13				
cnfg_ref_source_frequency (R/W)	_1	20	Set to zero			bucket_id_1		Set to zero			
	_2	21	Set to zero			bucket_id_2		Set to zero			
	3	22	divn_3	lock8k_3	bucket_id_3		reference_source_frequency_3				
	4	23	divn_4	lock8k_4	bucket_id_4		reference_source_frequency_4				
	5	24	divn_5	lock8k_5	bucket_id_5		reference_source_frequency_5				
	6	25	divn_6	lock8k_6	bucket_id_6		reference_source_frequency_6				
	7	26	divn_7	lock8k_7	bucket_id_7		reference_source_frequency_7				
	8	27	divn_8	lock8k_8	bucket_id_8		reference_source_frequency_8				
	9	28	divn_9	lock8k_9	bucket_id_9		reference_source_frequency_9				
	10	29	divn_10	lock8k_10	bucket_id_10		reference_source_frequency_10				
	11	2A	divn_11	lock8k_11	bucket_id_11		reference_source_frequency_11				
	12	2B	divn_12	lock8k_12	bucket_id_12		reference_source_frequency_12				
	13	2C	divn_13	lock8k_13	bucket_id_13		reference_source_frequency_13				
	14	2D	divn_14	lock8k_14	bucket_id_14		reference_source_frequency_14				
	cnfg_sts_remote_sources_valid (R/W)	30	FF	Remote status, channels <8:1>							
31		3F	Remote status, channels <14:9>								
cnfg_operating_mode (R/W)	32	00							TO_DPLL_operating_mode		

INTERNATIONAL AG FINAL PRODUCT BRIEF

Table 7 Register Map (cont...)

Register Name	Address (hex)	Default (hex)	Data Bit								
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
RO = Read Only R/W = Read/Write											
force_select_reference_source (R/W)	33	0F	forced_reference_source								
cnfg_input_mode (Bit 1 RO, otherwise R/W)	34	C2	auto_extsync_en	phalarm_timeout	XO_edge	man_holdover	extsync_en	IP_sonsdhb	master_slave	reversion_mode	
cnfg_T4_path (R/W)	35	40	Lock_T4_to_T0	T4_dig_feedback		T4_op_from_T0	T4_forced_reference_source				
cnfg_differential_inputs (R/W)	36	02								I6_PECL	I5_LVDS
cnfg_uPsel_pins (RO)	37	02	Microprocessor type								
cnfg_dig_outputs_sonsdh (R/W)	38	1F		dig2_sonsdh	dig1_sonsdh						
cnfg_digital_frequencies (R/W)	39	08	digital2_frequency		digital1_frequency						
cnfg_differential_outputs (R/W)	3A	C6					T07_PECL_LVDS		T06_LVDS_PECL		
cnfg_auto_bw_sel (R/W)	3B	FB	auto_BW_sel				T0_lim_int				
cnfg_nominal_frequency (R/W)	[7:0] 3C [15:8] 3D	99	Nominal frequency [7:0]								
cnfg_holdover_frequency (R/W)	[7:0] 3E [15:8] 3F	00	Holdover frequency [7:0]								
cnfg_holdover_modes (R/W)	40	88	auto_averaging	fast_averaging	read_average	Mini-holdover_mode	Holdover frequency [18:16] (with Registers 3E and 3F above)				
cnfg_DPLL_freq_limit (R/W)	[7:0] 41 [9:8] 42	76 00	DPLL frequency offset limit [7:0]							DPLL frequency offset limit[9:8]	
cnfg_interrupt_mask (R/W)	[7:0] 43 [15:8] 44 [23:16] 45	00	I8 interrupt not masked	I7 interrupt not masked	I6 interrupt not masked	I5 interrupt not masked	I4 interrupt not masked	I3 interrupt not masked	I2 interrupt not masked	I1 interrupt not masked	
			Operating_mode interrupt not masked	Main_ref_failed interrupt not masked	I14 interrupt not masked	I13 interrupt not masked	I12 interrupt not masked	I11 interrupt not masked	I10 interrupt not masked	I9 interrupt not masked	
			Sync_ip_alarm interrupt not masked	T4_status interrupt not masked	phasemon_alarm interrupt not masked	T4_inputs_failed interrupt not masked	AMI2_Viol interrupt not masked	AMI2_LOS interrupt not masked	AMI1_Viol interrupt not masked	AMI1_LOS interrupt not masked	
cnfg_freq_divn (R/W)	[7:0] 46 [13:8] 47	FF 3F	divn_value [7:0]								
cnfg_monitors (R/W)	48	05	freq_mon_clock	los_flag_on_TDO	ultra_fast_switch	ext_switch	PBO_freeze	PBO_en	freq_monitor_soft_enable	freq_monitor_hard_enable	
cnfg_freq_mon_threshold (R/W)	49	23	soft_frequency_alarm_threshold [3:0]				hard_frequency_alarm_threshold [3:0]				
cnfg_current_freq_mon_threshold (R/W)	4A	23	current soft frequency alarm threshold [3:0]				current hard frequency alarm threshold [3:0]				
cnfg_registers_source_select (R/W)	4B	00				T4_T0_select	frequency_measurement_channel_select [3:0]				
sts_freq_measurement (R/W)	4C	00	freq_measurement_value [7:0]								
cnfg_DPLL_soft_limit (R/W)	4D	8E	Freq limit Phase loss enable	DPLL Frequency Soft Alarm Limit [6:0] Resolution = 0.628 ppm							
cnfg_upper_threshold_0 (R/W)	50	06	Configuration 0: Activity alarm set threshold [7:0]								
cnfg_lower_threshold_0 (R/W)	51	04	Configuration 0: Activity alarm reset threshold [7:0]								
cnfg_bucket_size_0 (R/W)	52	08	Configuration 0: Activity alarm bucket size [7:0]								
cnfg_decay_rate_0 (R/W)	53	01								Cfg 0:decay_rate [1:0]	
cnfg_upper_threshold_1 (R/W)	54	06	Configuration 1: Activity alarm set threshold [7:0]								
cnfg_lower_threshold_1 (R/W)	55	04	Configuration 1: Activity alarm reset threshold [7:0]								
cnfg_bucket_size_1 (R/W)	56	08	Configuration 1: Activity alarm bucket size [7:0]								
cnfg_decay_rate_1 (R/W)	57	01								Cfg 1:decay_rate [1:0]	
cnfg_upper_threshold_2 (R/W)	58	06	Configuration 2: Activity alarm set threshold [7:0]								
cnfg_lower_threshold_2 (R/W)	59	04	Configuration 2: Activity alarm reset threshold [7:0]								
cnfg_bucket_size_2 (R/W)	5A	08	Configuration 2: Activity alarm bucket size [7:0]								
cnfg_decay_rate_2 (R/W)	5B	01								Cfg 2:decay_rate [1:0]	
cnfg_upper_threshold_3 (R/W)	5C	06	Configuration 3: Activity alarm set threshold [7:0]								
cnfg_lower_threshold_3 (R/W)	5D	04	Configuration 3: Activity alarm reset threshold [7:0]								
cnfg_bucket_size_3 (R/W)	5E	08	Configuration 3: Activity alarm bucket size [7:0]								
cnfg_decay_rate_3 (R/W)	5F	01								Cfg 3:decay_rate [1:0]	

Table 7 Register Map (cont...)

Register Name	Address (hex)	Default (hex)	Data Bit									
			7 (MSB)	6	5	4	3	2	1	0 (LSB)		
RO = Read Only R/W = Read/Write												
cnfg_output_frequency (R/W)												
(T01 & T02)	60	85	output_freq_2 (T02)				output_freq_1 (T01)					
(T03 & T04)	61	86	output_freq_4 (T04)				output_freq_3 (T03)					
(T05 & T06)	62	8A	output_freq_6 (T06)				output_freq_5 (T05)					
(T07 to T011)	63	F6	MFrSync enable	FrSync enable	T09 enable	T08 enable	output_freq_7 (T07)					
cnfg_T4_DPLL_frequency (R/W)	64	01		Auto Disable T4 output	AMI Duty cycle	T4 SONET/SDH selection	T4_DPLL_frequency					
cnfg_T0_DPLL_frequency (R/W)	65	01	T4 for measuring T0 phase	T4 APLL for T0 E1/DS1	T0 Freq to T4 APLL		T0_DPLL_frequency					
cnfg_T4_DPLL_bw (R/W)	66	00							T4_DPLL_bandwidth [1:0]			
cnfg_T0_DPLL_locked_bw (R/W)	67	0B							T0_DPLL_locked_bandwidth [4:0]			
cnfg_T0_DPLL_acq_bw (R/W)	69	0F							T0_DPLL_acquisition bandwidth [4:0]			
cnfg_T4_DPLL_damping (R/W)	6A	13	T4_PD2_gain_alog_8K [6:4]				T4_damping [2:0]					
cnfg_T0_DPLL_damping (R/W)	6B	13	T0_PD2_gain_alog_8K [6:4]				T0_damping [2:0]					
cnfg_T4_DPLL_PD2_gain (R/W)	6C	C2	T4_PD2_gain_enable	T4_PD2_gain_alog [6:4]			T4_PD2_gain_digital [2:0]					
cnfg_T0_DPLL_PD2_gain (R/W)	6D	C2	T0_PD2_gain_enable	T0_PD2_gain_alog [6:4]			T0_PD2_gain_digital [2:0]					
cnfg_phase_offset (R/W) [7:0]	70	00	phase_offset_value[7:0]									
[15:8]	71	00	phase_offset_value[15:8]									
cnfg_PBO_phase_offset (R/W)	72	00	PBO_phase_offset [5:0]									
cnfg_phase_loss_fine_limit (R/W)	73	A2	Fine limit Phase loss enable (1)	No activity for phase loss	Test Bit Set to 1			phase_loss_fine_limit [2:0]				
cnfg_phase_loss_coarse_limit (R/W)	74	85	Coarse limit Phase loss enable (2)	Wide range enable	Enable Multi Phase resp.	Phase loss coarse limit in UI pk-pk [3:0]						
cnfg_phasemon (R/W)	76	06	Input noise window enable		Phasemon Enable	Phasemon Auto PBO	Phase monitor limit [3:0]					
sts_current_phase (RO) [7:0]	77	00	current_phase[7:0]									
[15:8]	78	00	current_phase[15:8]									
cnfg_phase_alarm_timeout (RO)	79	32	Timeout value in 2s intervals [5:0]									
cnfg_sync_pulses (R/W)	7A	00	2 k/8 k out from T4				8 k invert	8 k pulse enable	2 k invert	2 k pulse enable		
cnfg_sync_phase (R/W)	7B	00	indep_FrSync/MFrSync	Sync_OC-N_rates				Sync_phase				
cnfg_sync_monitor (R/W)	7C	2B	ph_offset_ramp	Sync_monitor_limit			Sync_reference_source					
cnfg_interrupt (R/W)	7D	02					GPO interrupt enable	Interrupt tristate enable	Interrupt polarity enable			
cnfg_protection (R/W)	7E	85	protection_value									
cnfg_uPsel (R/W)	7F	02 *	Microprocessor type (*Default value depends on value on UPSEL[2:0] pins)									

Ordering Information

Table 8 Parts List

Part Number	Description
ACS8530	SETS Synchronous Equipment Timing Source for Stratum 2/3E Systems
ACS8530 EVB	Evaluation Board and Software

Disclaimers

Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Right to change- Changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

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