AN1200.23

Recommended SX1272 Settings for LoRaWAN Network Operation

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1 Introduction

This application note presents the recommended setup of the SX1272 radio transceiver operating in a LoRaWAN network.

2 Uplink Transmissions

2.1 LoRa Mode

Uplink transmissions can use the following LoRa settings:

1. LoRa modulation with 125 kHz bandwidth, SF7 to SF12.
2. LoRa modulation with 250 kHz bandwidth, SF7 only. Corresponding to the high speed channel

The following radio settings should be used:

SX1272 Register (address)	Register bit field (bit #)	Values	Note
RegOpMode (0x01)	LongRangeMode[7] Mode[2:0]	'1' '011'	LoRa mode enabled Tx mode
RegPaRamp (0x0A)	PaRamp[3:0]	'1000'	50 us PA Ramp-up time
RegModemConfig1 (0x1D)	Bw[7:6] CodingRate[5:3] ImplicitHeaderModeOn[2] RxPayloadCrcOn[1] LowDataRateOptimize[0]	'00' or '01' '001' '0' '1' '0' or '1'	'00' for 125kHz modulation Bandwidth '01' for 250kHz modulation Bandwidth 4/5 error coding rate Packets have up-front header CRC enable '0' when Spreading Factor is <= 10 '1' when Spreading Factor is >= 11
RegModemConfig2 (0x1E)	SpreadingFactor[7:4]	'0111' to '1100'	with 125kHz bandwidth : '0111' (SF7) = 6kbit/s '1100' (SF12) = 300 bit/s (only SF7 is supported with 250kHz bandwidth)
RegSyncWord (0x39)	LoRa sync word	0x34	Set sync word for LoRaWAN networks (default is 0x12 for other networks)
RegInvertIQ (0x33)	IQ inversion bits	0x27	This is the default value, no inversion
RegInvertIQ2 (0x3B)	IQ invertion bits	0x1d	This is the default value, no inversion

All registers not explicitly mentioned can stay with their default value.

2.2 GFSK Mode

The LoRaWAN specification defines a high speed uplink channel using 50kbit/s GFSK modulation. The following radio settings should be used (all settings omitted should be left to their default value)

General and Transmitter settings

- Modulation = FSK
- Fdev = +/-25kHz (modulation index = 1)
- Bit rate setting = 50kbit/s
- Gaussian filter ON
- Filter setting : BT=0.5
- Output Power setting: hardware dependent
- PA selection: hardware dependent

SX1272 Register (address)	Register bit field (bit #)	Values	Note
RegOpMode (0x01)	LongRangeMode[7] ModulationType[6:5] ModulationShaping[4:3] Mode[2:0]	'0' '00' '10' '011'	FSK/OOK mode enable FSK Modulation scheme Gaussian filter BT = 0.5 Tx mode
RegBitrateMsb (0x02)	BitRate[15:8]	0x02	BitRate set to 50kbps
RegBitrateLsb (0x03)	BitRate[7:0]	0x80	
RegFdevMsb (0x04)	Fdev[13:8]	0x01	Frequency deviation set to +/-25kHz
RegFdevLsb (0x05)	Fdev[7:0]	0x99	

Frame and Packet Handler settings

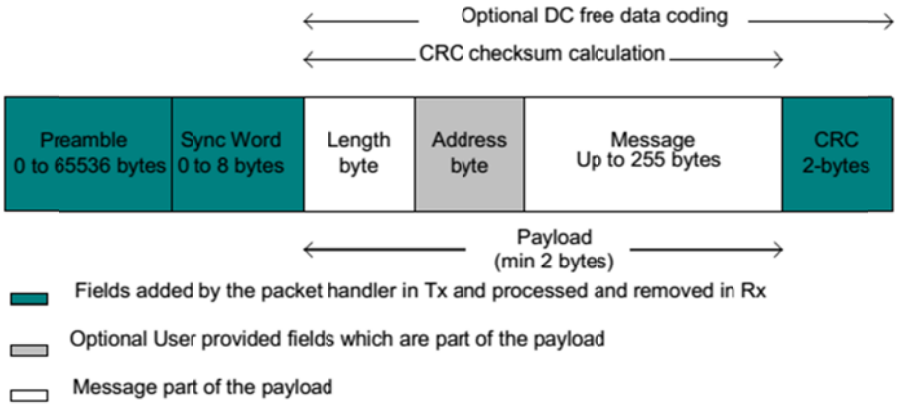

Figure 1: Packet Handler Format

- Packet Mode : this mode inserts a PHY header to support variable payload length
- Preamble Length = 5 bytes
- Sync Word= 3 bytes : 0xC194C1
- Variable Length frame format
- DC-free data encoding = Whitening
- CrcOn=1, CrcAutoclearOn=1

SX1272 Register (address)	Register bit field (bit #)	Values	Note
RegPreambleMsb (0x25)	PreambleSize[15:8]	0x00	5 Byte of preamble for each packet
RegPreambleLsb (0x26)	PreambleSize[7:0]	0x05	
RegSyncConfig (0x27)	AutoRestartRxMode[7:6]	'00'	AutoRestart OFF
	PreamblePolarity[5]	'0'	Preamble 0xAA
	SyncOn[4]	'1'	Sync Address enable
	FifoFillCondition[3]	'0'	Fill FIFO when Sync Address is detected
	SyncSize[2:0]	'002'	3 Bytes of Sync Word
RegPacketConfig1 (0x30)	PacketFormat[7]	'1'	Variable length packets
	DcFree[6:5]	'10'	Whitening encoding enable
	CrcOn[4]	'1'	Enable CRC calculation
	CrcAutoClearOff[3]	'0'	Clear FIFO when CRC check fails
	AddressFiltering[2:1]	'00'	No address filtering
	CrcWhiteningType[0]	'0'	CCITT CRC and Whitening implementation
RegPacketConfig2 (0x31)	DataMode[6]	'1'	Packet Mode
RegSyncValue1 (0x28)	SyncValue[63:56]	0xC1	Sync Address is 0xC194C1
RegSyncValue2 (0x29)	SyncValue[55:48]	0x94	
RegSyncValue2 (0x2A)	SyncValue[47:40]	0xC1	

3 Downlink Reception Slots Following an Uplink

A LoRaWAN node opens two reception slots for potential downlink communications after each uplink transmissions. The delay between the end of a transmission (signaled by the TxDone IRQ) and the beginning of the reception slot is constant and defined extremely precisely to minimize the reception current overhead on the end-point side. Most of the time this reception slot will not be used by the gateways, id no frame will be received. Therefore, to minimize the current consumption the radio is programmed to listen to the channel for the minimum time required to detect with certainty the presence or absence of a preamble. In the absence of a preamble, the radio goes back to stand-by mode.

3.1 LORA Mode

3.1.1 Register Settings

In LoRa mode this is achieved simply by using the Receive Single mode, with “IQ inversion”

SX1272 Register (address)	Register bit field (bit #)	Values	Note
RegOpMode (0x01)	LongRangeMode[7] Mode[2:0]	‘1’ ‘110’	LoRa mode enable Receive Single mode
RegLna (0x0C)	LnaGain[7:5] LnaBoost[1:0]	‘001’ ‘11’	LNA gain set to the maximum value LNA Boost enable
RegModemConfig1 (0x1D)	Bw[7:6] CodingRate[5:3] ImplicitHeaderModeOn[2] RxPayloadCrcOn[1] LowDataRateOptimize[0]	‘00’ or ‘01’ ‘001’ ‘0’ ‘1’ ‘0’ or ‘1’	‘00’ for 125kHz modulation Bandwidth ‘01’ for 250kHz modulation Bandwidth 4/5 error coding rate Packet have up-front header CRC enable ‘0’ when Spreading Factor is <= 10 ‘1’ when Spreading Factor is >= 11
RegModemConfig2 (0x1E)	SpreadingFactor[7:4] AgcAutoOn[2] SymbTimeout[1:0]	‘0111’ to ‘1100’ ‘1’ ‘00’	with 125kHz bandwidth: ‘0111’ (SF7) = 6kbit/s ‘1100’ (SF12) = 300 bit/s (only SF7 is supported with 250kHz bw) LNA gain set by internal AGC loop
RegSymbTimeoutLsb (0x1F)	SymbTimeout[7:0]	0x05 or 0x08	0x05 when Spreading Factor is >= 10 0x08 when Spreading Factor is <= 9 Length of the receiver window in symbols. If no preamble is detected during this time , the receiver goes back to stand-by
RegMaxPayloadLength (0x23)	PayloadMaxLength[7:0]	0x40	Sets the maximum possible downlink payload size to 64 bytes. Packets with payload greater than this threshold will not be demodulated, receiver will immediately go back to “stand-by” low power mode
RegSyncWord (0x39)	LoRa sync word	0x34	Set sync word for LoRaWAN networks (default is 0x12 for other networks)
RegInvertIQ (0x33)	IQ inversion bits	0x67	Optimised for inverted IQ
RegInvertIQ2 (0x3B)	IQ invertion bits	0x19	Optimised for inverted IQ

Note: settings related to IQ inversion must be reverted back to their default value for uplink transmission.

3.1.2 RX Window Precise Timing

This paragraph explains the optimal RX start-up time and RX slot duration for the given timing precision reachable by the end-device.

The downlink preamble transmitted by the gateways contains 8 symbols. The receiver requires 5 symbols to detect the preamble and synchronize. Therefore there must be a 5 symbols overlap between the receive window and the transmitted preamble.

The gateway always initiates the transmission of the preamble 1 sec +/- 20uSec after the end of the uplink. Therefore the beginning of the downlink preamble can be considered as a perfectly precise reference for the rest of this calculation.

Notation:

BW	Signal modulation bandwidth in Hz
SF	LORA spreading factor : 7 to 12
Tsymb	Duration of a LORA symbol = $\frac{2^{SF}}{BW}$ sec
RXwindow	Length of the receive window
RXoffset	Offset in sec between the optimal receiver turn-on time and the actual start of the gateway transmission
RXerror	Maximum timing error of the receiver. The receiver will turn-on in a [-RXerror : +Rxerror] sec interval around RXoffset
T_RX_early	Earliest time at which the receiver can start and synchronize on the downlink preamble
T_RX_late	Latest time at which the receiver can start and synchronize on the downlink preamble

Those variables are illustrated in the following diagram:

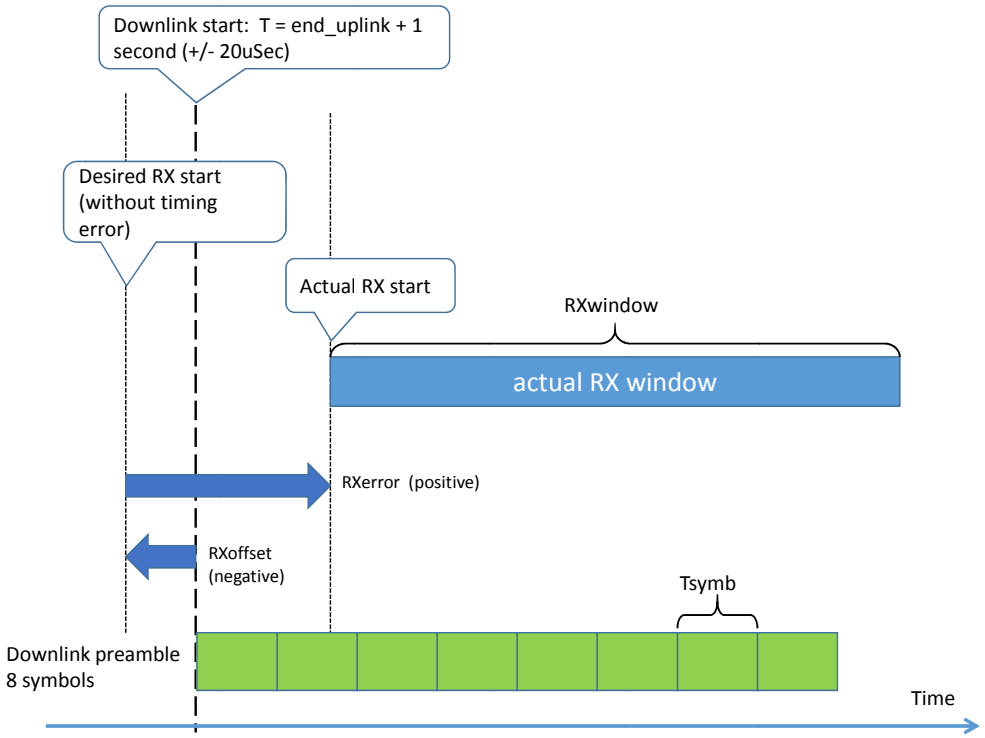

Figure 2: Typical Rx Window Timing

The following diagram illustrates the positioning of the earliest and latest possible receive windows to achieve 5 overlapping symbols with the downlink preamble:

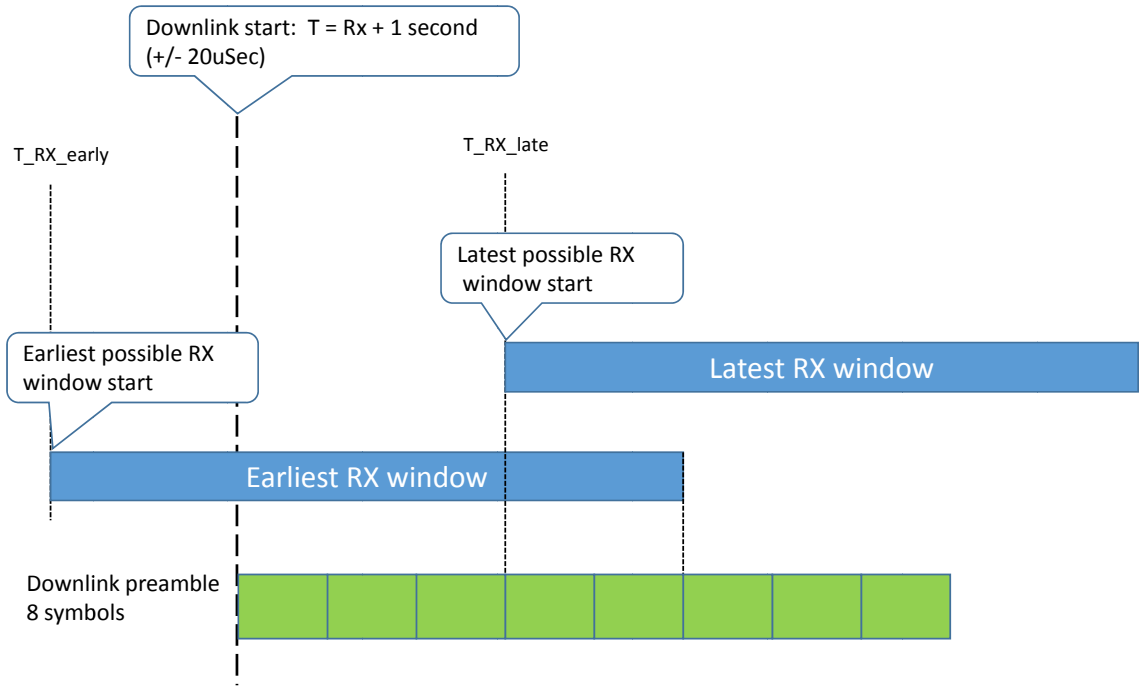

Figure 3: Worst Case Rx Window Timings

From this diagram the following equation can be deduced:

- T_RX_late = 3 x Tsymb
- T_RX_early = 5 x Tsymb – RXwindow

Additionnaly the difference between T_RX_late and T_RX_early corresponds to the maximum timing error range of the receiver therefore:

- T_RX_late – T_RX_early = 2 x RXerror

To allow this maximum timing error range the receiver should be programmed to ideally turn-on at the mid-point between T_RX_late and T_RX_early , therefore:

- RXoffset = (T_RX_late + T_RX_early)/2

So assuming the RXerror parameter is set (RXerror is a direct consequence of a given design, it depends on the oscillator precision, temperature drift, …)
We can deduce:

- RXwindow = 2 x Tsymb + 2 x RXerror
- RXoffset = 4 x Tsymb – Rxwindow/2

Because the minimum RXwindow must be at least 5 symbols long, the system always tolerates at least an RXerror of at least 1.5 x Tsymb

Numerical application:

The sensor can achieve a +/- 1.5mSec timing drift after a 1sec sleep period and is using SF7/125kHz

At SF7/125kHz Tsymb = 1mSec

So we set RXerror = 1.5mSec

We deduce RXwindow = 2 x Tsymb + 2 x RXerror

= 2 x 128 / 125e3 + 3e-3 = 5mSec

The RXwindow is expressed in symbol unit in the SX1272 transceiver, at SF7 a symbol is 1mSec long therefore the RWwindow corresponds to 5 symbols.

The sensor will programmed to start with RXoffset = 4 x Tsymb – RXwindow/2

= 4e-3 – 2.5e-3 = 1.5e3.

Without timing error, the receiver should turn on exactly 1.5mSec after the beginning of the downlink preamble.

The sensor can achieve a +/- 20mSec timing drift after a 1sec sleep period and is using SF7/125kHz

RXwindow = 2 x Tsymb + 2x RXerror = 42mSec , this is larger than 5 symbols , therefore we set RXwindow to the immediatemy greater or equal length which is an integer multiple of Tsymb

- RXwindow = 42 x Tsymb = 42mSec

Then:

- RXoffset = 4 x Tsymb – RXwindow/2 = -17mSec

The receiver should be programmed to start 17mSec before the start of the downlink preamble

The same sensor but now using SF10/125kHz instead of SF7

At SF10/125kHz Tsymb = 8.2mSec

RXwindow = 2 x Tsymb + 2x RXerror = 56.4mSec , this is larger than 5 symbols , therefore we set RXwindow to the immediately greater or equal length which is an integer multiple of Tsymb

- RXwindow = 7 x Tsymb = 57.4mSec

Then:

- RXoffset = 4 x Tsymb – RXwindow/2 = 4.1mSec

The receiver should be programmed to start 4.1mSec after the start of the downlink preamble

The following tables give a few numerical examples for various SF / BW/ timing error sets:

Rxerror +/- 1.5 mSec
BW 125 kHz

SF	Tsymb (mSec)	RXoffset (mSec)	RX window Symb	RX window mSec
7	1.0	1.5	5.0	5.1
8	2.0	3.1	5.0	10.2
9	4.1	6.1	5.0	20.5
10	8.2	12.3	5.0	41.0
11	16.4	24.6	5.0	81.9
12	32.8	49.2	5.0	163.8

Rxerror +/- 20 mSec
BW 250 kHz

SF	Tsymb (mSec)	RXoffset (mSec)	RX window Symb	RX window mSec
7	0.5	-18.7	81.0	41.5
8	1.0	-17.4	42.0	43.0
9	2.0	-14.3	22.0	45.1
10	4.1	-8.2	12.0	49.2
11	8.2	4.1	7.0	57.3
12	16.4	24.6	5.0	81.9

Rxerror +/- 20 mSec
BW 250 kHz

SF	Tsymb (mSec)	RXoffset (mSec)	RX window Symb	RX window mSec
7	0.5	-18.7	81.0	41.5
8	1.0	-17.4	42.0	43.0
9	2.0	-14.3	22.0	45.1
10	4.1	-8.2	12.0	49.2
11	8.2	4.1	7.0	57.3
12	16.4	24.6	5.0	81.9

3.2 GFSK Mode

3.2.1 Register Settings

Receiver-specific settings

- RxBw=50kHz // single side Carson BW=50kHz
- AfcBw=83.3kHz // assuming +/-30ppm of LO misalignment at 869.525 MHz
- AgcAuto=On
- Preamble Detection On, over 2 Bytes, Number of samples in error = 10
- AfcAutoOn
- AfcAutoClearOn
- RxTrigger=Preamble
- LnaBoost=On

SX1272 Register (address)	Register bit field (bit #)	Values	Note
RegLna (0x0C)	LnaGain[7:5] LnaBoost[1:0]	'001' '11'	LNA gain set to the highest gain LNA Boost enable
RegRxConfig (0x0D)	RestartRxOnCollision[7] RestartRxWithoutPllLock[6] RestartRxWithPllLock[5] AfcAutoOn[4] AgcAutoOn[3] RxTrigger[2:0]	'0' '0' '0' '1' '1' '110'	No restart on collision Corrects frequency offset Automatic gain control Trigs on preamble only
RegRxBw (0x12)	RxBwMant[4:3] RxBwExp[2:0]	'01' '011'	Receiver Bandwidth =50kHz SSB
RegAfcBw (0x13)	RxBwMantAfc[4:3] RxBwExpAfc[2:0]	'10' '010'	Receiver Bandwidth =83.3kHz SSB for AFC
RegPreambleDetect (0x1F)	PreambleDetectorOn[7] PreambleDetectorSize[6:5] PreambleDetectorTol[4:0]	'1' '01' '01010'	Preamble detector enable Preamble detection over 2 bytes 10 chip errors tolerated over detection
RegSyncConfig (0x27)	AutoRestartRxMode[7:6] PreamblePolarity[5] SyncOn[4] FifoFillCondition[3] SyncSize[2:0]	'00' '0' '1' '0' '002'	AutoRestart OFF Preamble 0xAA Sync Address enable Fill FIFO when Sync Address is detected 3 Bytes of Sync Word
RegPacketConfig1 (0x30)	PacketFormat[7] DcFree[6:5] CrcOn[4] CrcAutoClearOff[3] AddressFiltering[2:1] CrcWhiteningType[0]	'1' '10' '1' '1' '00' '0'	Variable length packets Whitening encoding enable Enable CRC calculation PayloadReady IRQ will always be generated at the end of the frame, CRC must be checked through dedicated flag No address filtering CCITT CRC and Whitening implementation
RegPacketConfig2 (0x31)	DataMode[6]	'1'	Packet Mode
RegSyncValue1 (0x28)	SyncValue[63:56]	0xC1	Sync Address is 0xC194C1
RegSyncValue2 (0x29)	SyncValue[55:48]	0x94	
RegSyncValue2 (0x2A)	SyncValue[47:40]	0xC1	

Expected performance: @ BER=0.1% = -109dBm (confirmed with PER on a short packet)

Operation Flowchart for Receiver

The following flowchart shows how the receiver should be operated for each reception slot in GFSK mode.

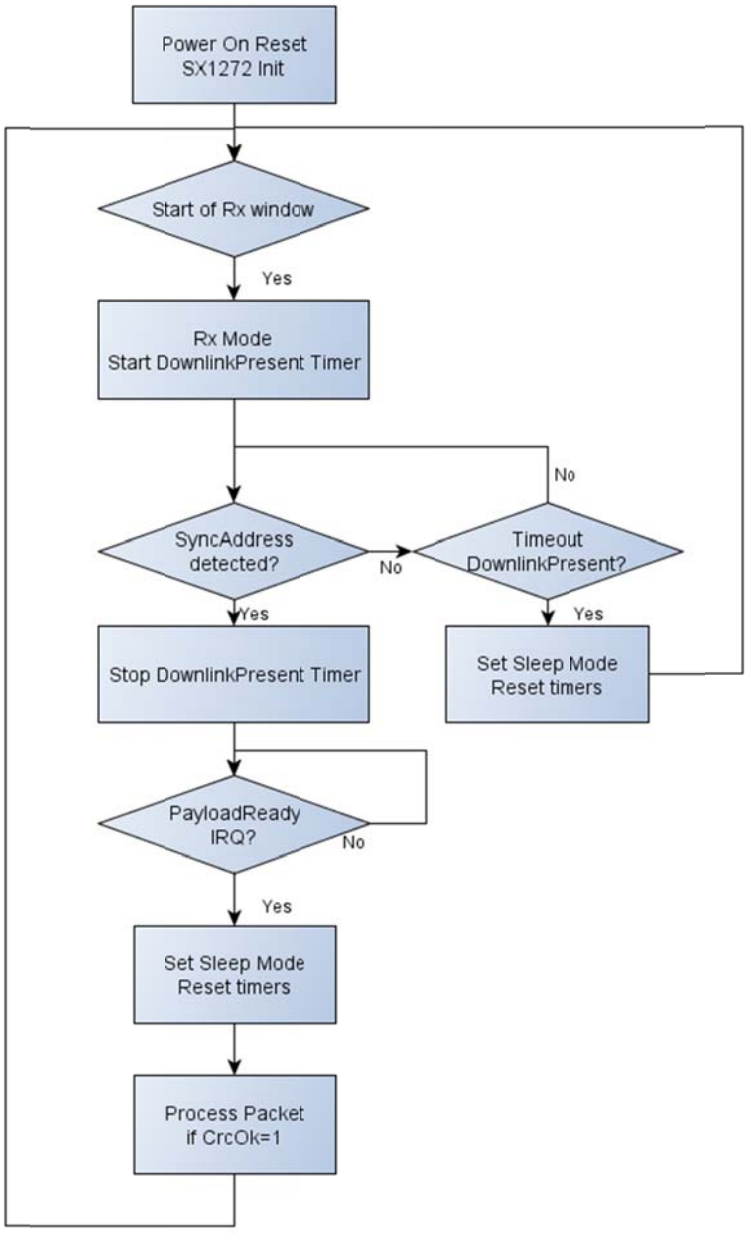

Figure 4: FSK Rx Operation Flowchart

DownlinkPresent timeout : timer started when the device is set to Rx mode. Sized to only leave the receiver open for a short amount of time when the downlink command is expected. It is meant to capture 5 bytes of Preamble + 3 Bytes of Sync Word + margin, so should be set to 1.3ms.

The *"SyncAddress"* interupt can be mapped to the DIO2 line of the SX1272 or can alternatively be polled through the SPI interface.

The *"PayloadReady"* interrupt can be mapped to the DIO0 line of the SX1272 or polled through the SPI interface.

3.2.2 RX Window Precise Timing in GFSK Mode

We note FSKbitrate the bit rate of the GFSK modulation in bit per sec

The GFSK frame preamble is 8 bytes long (5 bytes preamble + 3 bytes sync word), therefore the RX window and the beginning of the TX preamble must overlap on 8*8/FSKbitrate sec
The LoRaWAN v3 only supports a single GFSK bit rate = 50kbits/sec
Therefore the overlap must be equal or greater than 1.3mSec

So using the same notation than in the LORA section we have:

- T_RX_late = 0
- T_RX_early = 1.3mSec – RXwindow

Similarly we can deduce that for 50kbit/sec GFSK the minimal RXwindow is:

- RXwindow = 1.3mSec + 2 x RXerror

and

- RXoffset = – Rxwindow/2

4 Random Number Generation for Cryptography

The LoRaWAN MAC software layer requires the generation of truly random numbers for cryptography purposes. This can be achieved using the naturally random noise of the radio channel. The recommended way to generate a random binary number is the following:

Radio receiver settings:

SX1272 Register (address)	Register bit field (bit #)	Values	Note
RegOpMode (0x01)	LongRangeMode[7] Mode[2:0]	'1' '101'	LoRa mode enable Receive Continuous mode
RegModemConfig1 (0x1D)	Bw[7:6] CodingRate[5:3] ImplicitHeaderModeOn[2] RxPayloadCrcOn[1] LowDataRateOptimize[0]	'00' '001' '0' '1' '0'	'00' for 125kHz modulation Bandwidth 4/5 error coding rate Packet have up-front header CRC enable '0' when Spreading Factor is <= 10
RegModemConfig2 (0x1E)	SpreadingFactor[7:4] AgcAutoOn[2] SymbTimeout[1:0]	'0111' '1' '00'	'0111' (SF7) = 6kbit/s

To generate an N bit random number, perform N read operation of the register RegRssiWideband (address 0x2c) and use the LSB of the fetched value. The value from RegRssiWideband is derived from a wideband (4MHz) signal strength at the receiver input and the LSB of this value constantly and randomly changes.

The RegRssiValue register (at address 0x1b) should not be used for random number generation. It has been experimentally measured that if a constant CW input power is applied at the receiver input inside the current receiver channel the LSB of the RegRssiValue register may be constant or strongly biased.

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